WR0603

Ultra-low power consumption, CMOS LDO

1. General Descriptions

The WR0603 series low-power, low-dropout, CMOS linear voltage regulators operate from a 2.0V to 5.5V input voltage and deliver up to 600mA output current. They are the perfect choice for low voltage, low power applications. A low ground current makes this part attractive for battery operated power systems. The WR0603 series also offer low dropout voltage to prolong battery life in portable electronics.

The WR0603 series include a 10nA logic - controlled shutdown mode, short current limit and thermal shutdown protection. The WR0603 has auto-discharge function to quickly discharge V_{OUT} in the disable status.

The WR0603 series regulators are available in SOT23-5, DFN2*2-6L packages. Standard products are Pb-free and Halogen free products.

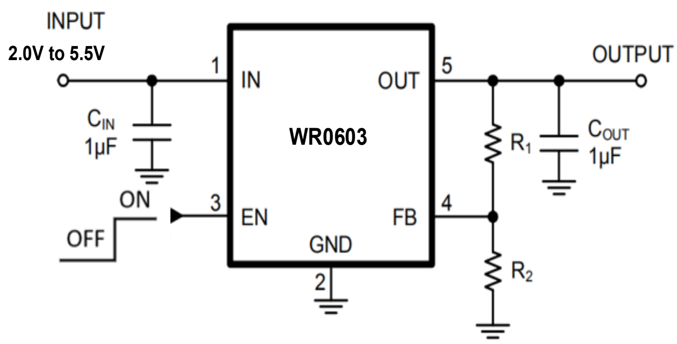
2. Features

- Low Dropout Voltage
- Thermal Overload Protection
- Built-In Fold Back Protection Circuit
- 25μA Low Ground Current
- 10nA Logic-Controlled Shutdown
- 2.0V to 5.5V Input Voltage Range
- Adjustable Output from 0.8V to 5.0V
- Short Auto-Discharge Function
- Quick Start-Up Time
- Operating Temperature: -40 to +85ºC
- Output short protection
- Quiescent Current: 25μA Typ.
- Recommend Capacitor: 1μF or more

3. Applications

- MP3/MP4 Players
- Cellphones, radiophone, digital cameras
- Bluetooth, wireless handsets
- Others portable electronic device

4. Typical Application

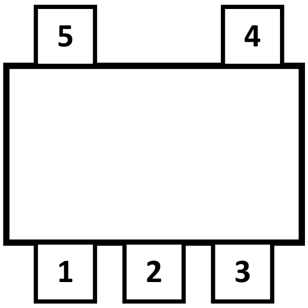


NOTE:Choose R_2=160kΩ to maintain a 5μA minimum load.
Calculate the value for R_1 using the following equation:

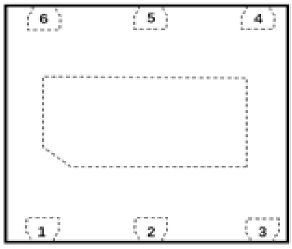
$$R_1 = R_2 * \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

5. Pin Configuration

(Top View)



SOT23-5



DFN2*2-6L

6. Pin Description

PIN Number		PIN NAME	I/O	PIN FUNCTIONS
SOT23-5	DFN2*2-6L			
1	3	IN	I	Input voltage supply. Bypass with a typical 1μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.
2	2	GND	-	Common ground.
3	1	EN	I	Enable input. Active High. EN is low when suspended.
4	6	FB	-	Feedback Pin
5	4	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 1μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 80Ω (typical) pull-down resistor prevents a charge from remaining on V_{OUT} when the regulator shutdowns.
-	5	NC	-	NC.

7. Absolute Maximum Ratings[1]

PARAMETER		RATING	UNIT
Input voltage range		-0.3 to 6.0	V
EN Input voltage range		-0.3 to V_{IN}	V
Output voltage range		-0.3 to V_{IN}	V
Power Dissipation [1][4] PD @T_A = 25ºC	SOT23-5	500	mW
	DFN2*2-6L	606	mW
Thermal Resistance, θ_{JA}	SOT23-5	250 [1]	ºC/W
		190 [2]	ºC/W
	DFN2*2-6L	165 [1]	ºC/W
		125 [2]	ºC/W
Top Thermal resistance $R_{\theta JC}$ [1][3]	SOT23-5	120	ºC/W
Junction Temperature		150	℃
Lead Temperature Range		260	℃
Storage Temperature Range		-65 to 150	℃
ESD Susceptibility	HBM	±4000	V

NOTE1: Measured on 2cm x 2cm 2-layer FR4 PCB board, 1 oz copper, no via holes on GND copper.
NOTE2: Measured on 2cm x 2cm 4-layer FR4 PCB board, 1 oz copper, no via holes on GND copper.
NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.
NOTE4: Power dissipation is calculated by $P_{D(MAX)} = (T_J - T_A) / R_{\theta JA}$.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	2.0 to 5.5	V
EN Input voltage range	0 to 5.5	V
Nominal output voltage range	0.8 to 5.0	V
Output current	0 to 600	mA
Input capacitor	1	μF
Output capacitor	1	μF
Operating temperature range	-40 to 85	℃

9. Electrical Characteristics (V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, Full= -40℃ to 85℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage			2.0		5.5	V
V_{OUT}	Output Voltage	I_{OUT}=1mA, T_A=+25ºC		0.98 V_{OUT}	V_{OUT}	1.02 V_{OUT}	V
		I_{OUT}=1mA , Full		0.975 V_{OUT}	V_{OUT}	1.025 V_{OUT}	
V_{FB}	Feedback Voltage	I_{OUT}=1mA, Full		0.784	0.8	0.816	V
I_{OUT}	Maximum Output Current	0.8V ≤ V_{OUT} < 1.2V, T_A=+25ºC		300			mA
		V_{IN}=V_{OUT}+1.0V, 1.2V ≤ V_{OUT} < 5.0V, T_A=+25ºC		600			
I_{LIM}	Current Limit	V_{EN}=V_{IN}, V_{OUT}=$V_{(normal)}$*95%, Full		700	750		mA
I_{SHORT}	Short Current	V_{EN}=V_{IN}, V_{OUT}=0V, Full			350		mA
I_Q	Quiescent Current	V_{EN} = V_{IN} , I_{OUT}=0mA, Full			25	40	μA
V_{DROP}	Dropout Voltage[1]	I_{OUT} = 300mA, Full	V_{OUT} = 0.8V		940	1200	mV
			V_{OUT} = 0.9V		840	1100	
			1.0V ≤ V_{OUT} < 1.1V		780	1000	
			1.1V ≤ V_{OUT} < 1.2V		680	900	
			1.2V ≤ V_{OUT} < 1.5V		590	800	
			1.5V ≤ V_{OUT} < 1.8V		420	550	
			1.8V ≤ V_{OUT} < 2.1V		320	420	
			2.1V ≤ V_{OUT} < 2.5V		260	340	
			2.5V ≤ V_{OUT} < 3.0V		215	280	
			3.0V ≤ V_{OUT} < 3.6V		190	250	
			3.6V ≤ V_{OUT} ≤ 5.0V		165	210	
		I_{OUT} = 600mA, Full	1.2V ≤ V_{OUT} < 1.5V		650	850	
			1.5V ≤ V_{OUT} < 1.8V		580	750	
			1.8V ≤ V_{OUT} < 2.1V		500	650	
			2.1V ≤ V_{OUT} < 2.5V		450	570	
			2.5V ≤ V_{OUT} < 3.0V		400	530	
			3.0V ≤ V_{OUT} < 3.6V		380	490	
			3.6V ≤ V_{OUT} ≤ 5.0V		330	420	

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LNR	Line Regulation	$V_{IN}=V_{OUT}+1.0V$ to 5.5V, $I_{OUT}=1mA$, $T_A=+25°C$		0.01	0.2	%/V
LDR	Load Regulation[2]	$I_{OUT}=1\sim600mA$, $T_A=+25°C$		10		mV
I_{SHDN}	Shut-down Current	$V_{EN}=0V$， $T_A=+25°C$		0.01	1	μA
PSRR	Power Supply Ripple Rejection	$V_{IN}=(V_{OUT}+1V)_{DC}+0.5V_{P-P}$ f=100Hz, $I_{OUT}=30mA$, $T_A=+25°C$		70		dB
		$V_{IN}=(V_{OUT}+1V)_{DC}+0.5V_{P-P}$ f=1kHz, $I_{OUT}=30mA$, $T_A=+25°C$		50		
V_{NO}	Output noise voltage	BW=10Hz to 100kHz, $V_{OUT}=1.8V$, $I_{OUT}=10mA$, $T_A=+25°C$		150		μV_{RMS}
V_{IH}	EN logic high voltage	$V_{IN}=5.5V$, $I_{OUT}=1mA$, Full	1.2			V
V_{IL}	EN logic low voltage	$V_{IN}=5.5V$, $I_{OUT}=1mA$, Full			0.4	V
I_{EN}	EN Input leakage	$V_{EN}=0V$ or 5.5V, Full	-1		1	μA
R_{DIS}	Output Discharge resistance	$V_{IN}=4.0V$, $V_{EN}=0V$, $T_A=+25°C$		80		Ω
T_C	Output Voltage Temperature Coefficient	$-40°C \le T_A \le 85°C$		100		ppm/°C
T_{SD}	Thermal shutdown threshold			140		°C
ΔT_{SD}	Thermal shutdown hysteresis			15		°C

Note1: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$ * 98%.
Note2: The Load regulation is measured using pulse techniques with duty cycle < 5%.

10. Typical Performance Characteristics (T_A= -40 to 85ºC, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

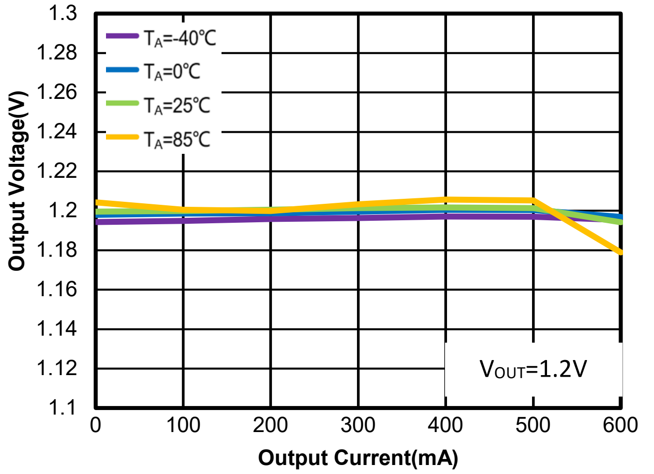


Figure 1. WR0603-ADA50R
Output Voltage vs. Output Current

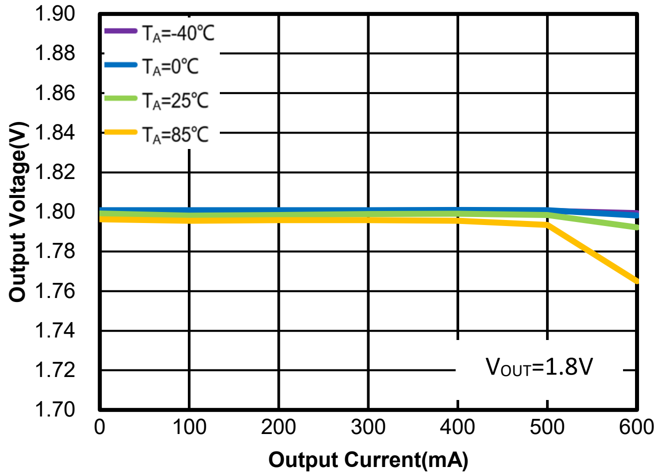


Figure 2. WR0603-ADA50R
Output Voltage vs. Output Current

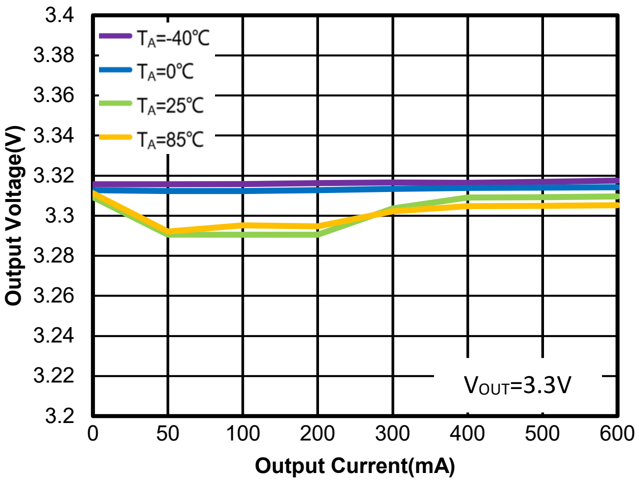


Figure 3. WR0603-ADA50R
Output Voltage vs. Output Current

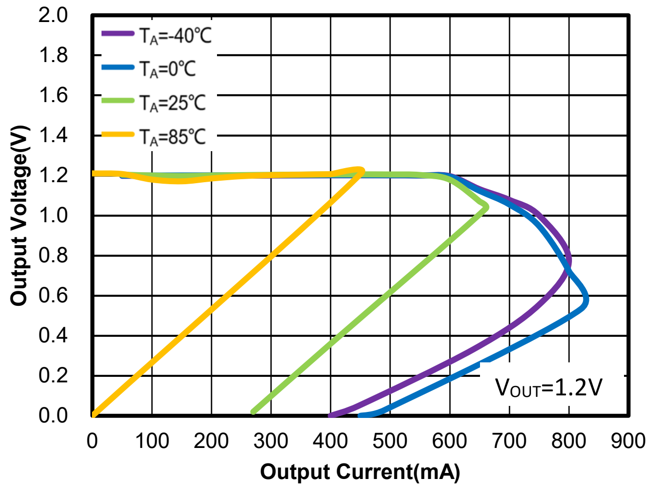


Figure4. WR0603-ADA50R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

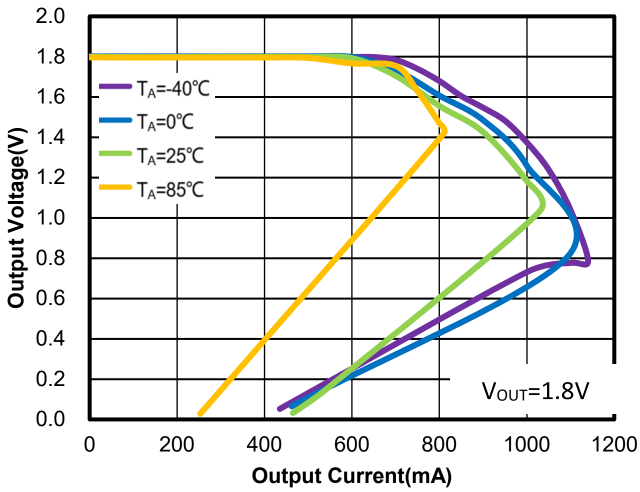


Figure 5. WR0603-ADA50R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

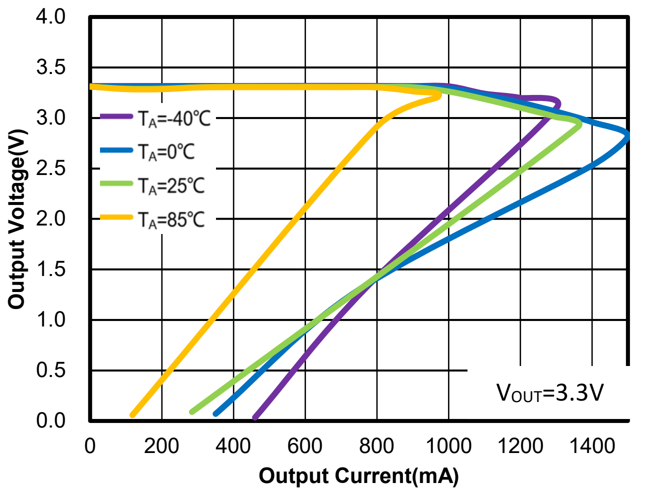


Figure 6. WR0603-ADA50R
Foldback Current Limit vs I_{OUT} & Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85°C, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

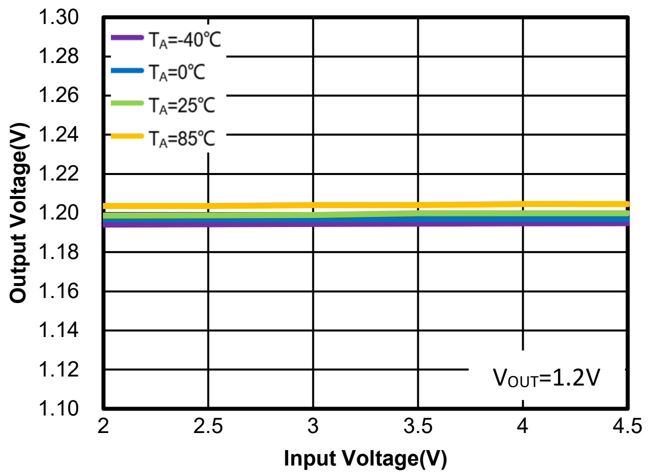


Figure 7. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

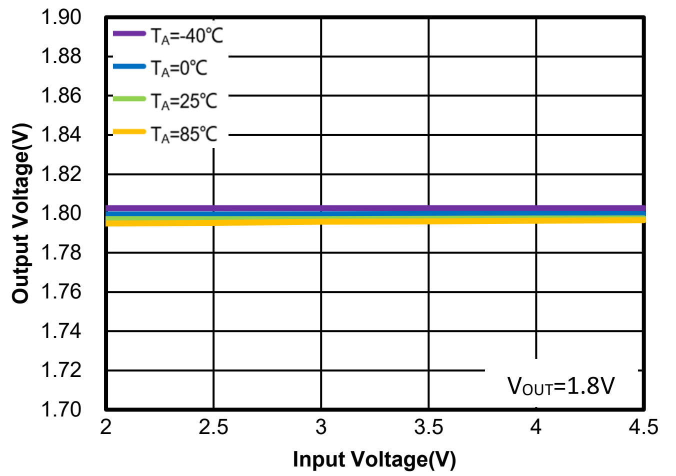


Figure 8. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

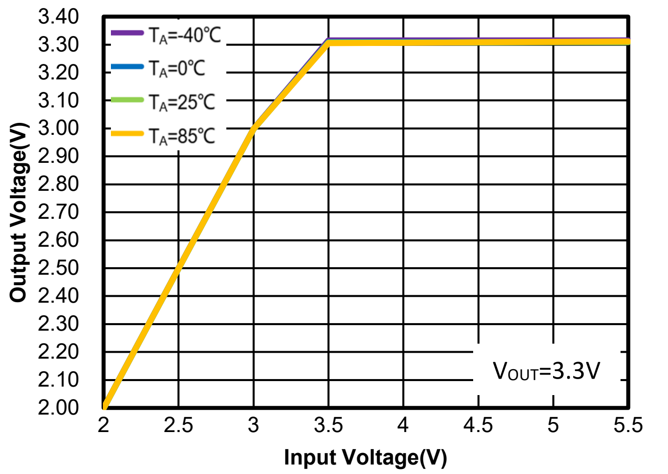


Figure9. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

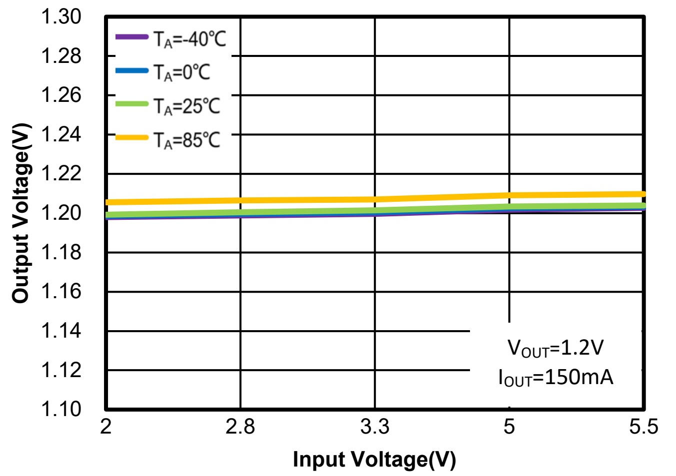


Figure10. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

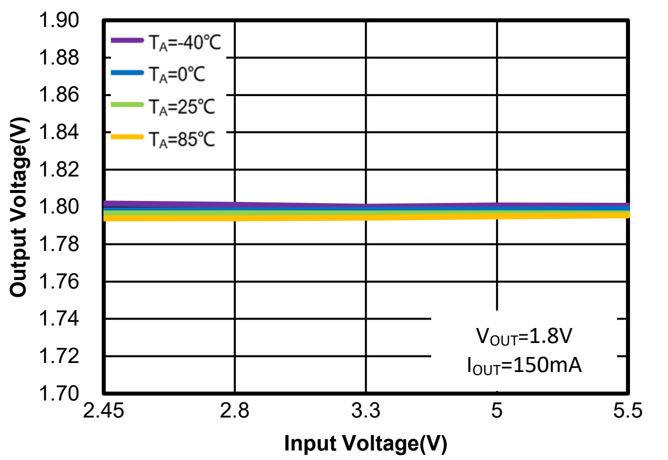


Figure11. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

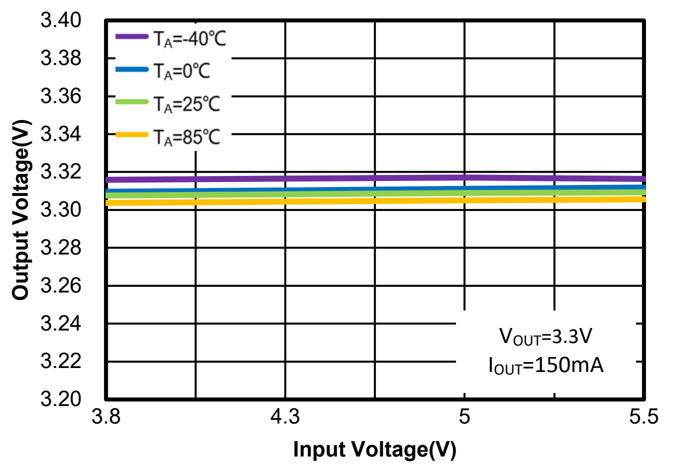


Figure12. WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

Typical Performance Characteristics
(T_A= -40 to 85ºC, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

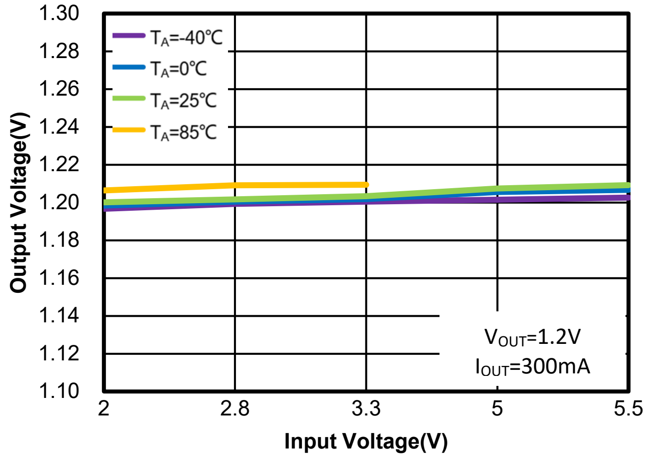


Figure13.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

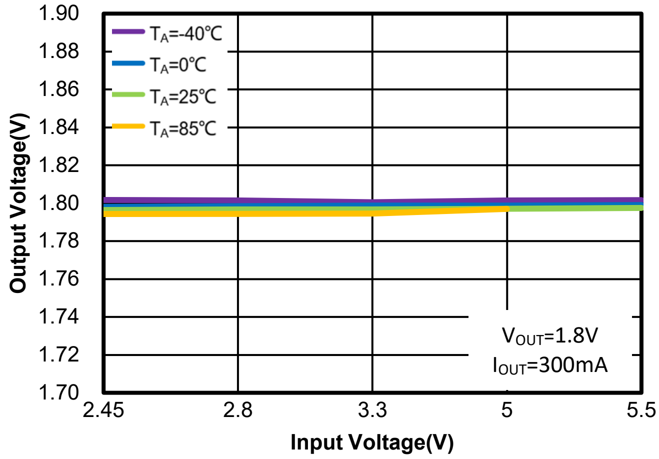


Figure14.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

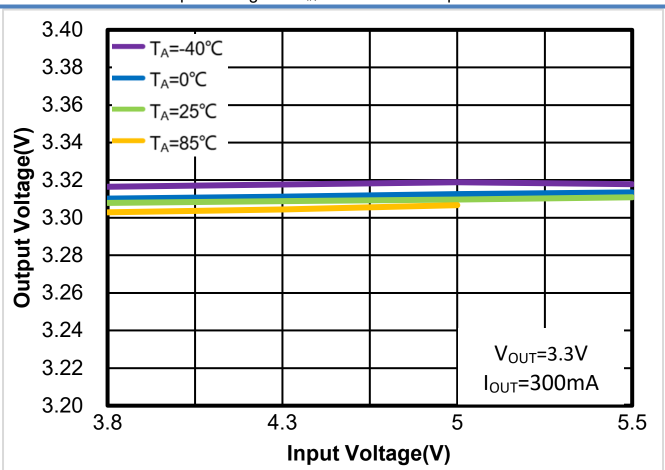


Figure15.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

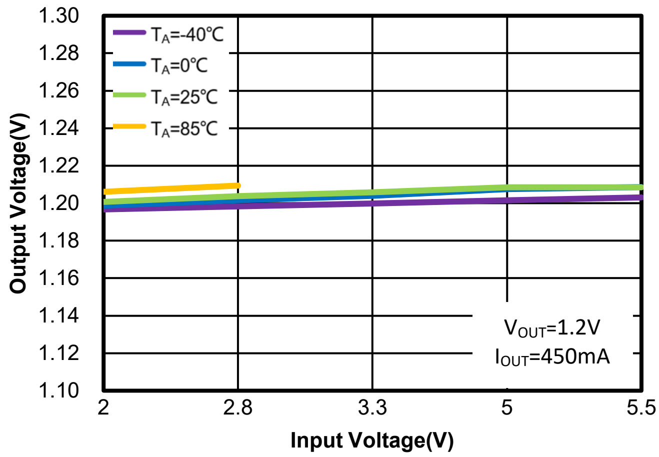


Figure16.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

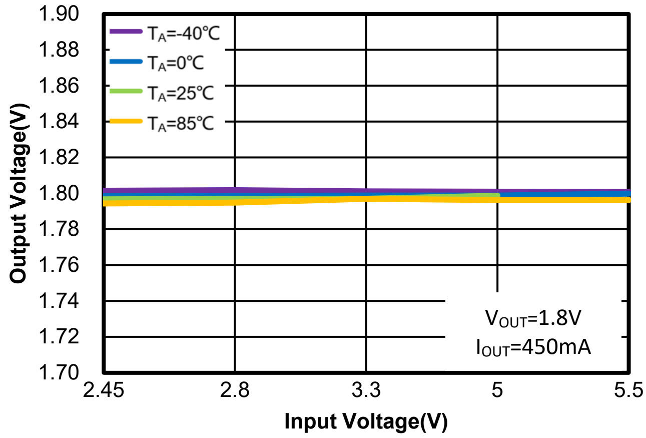


Figure17.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

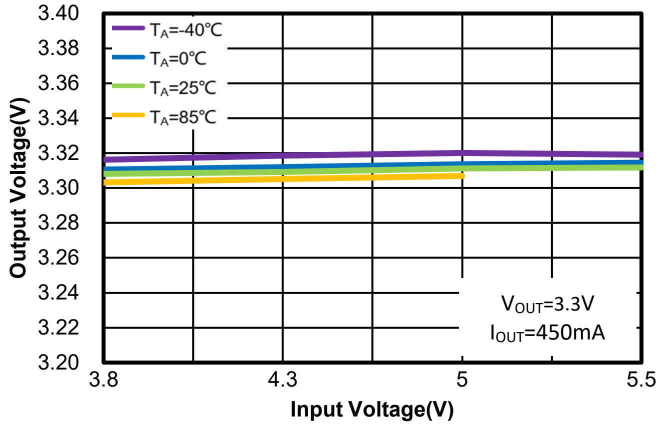


Figure18.WR0603-ADA50R
Output Voltage vs V_{IN} & Ambient Temperature

Typical Performance Characteristics (TA= -40 to 85ºC, VIN=VOUT+0.5V or 2.0V,whichever is greater, CIN=COUT=1μF, unless otherwise noted)

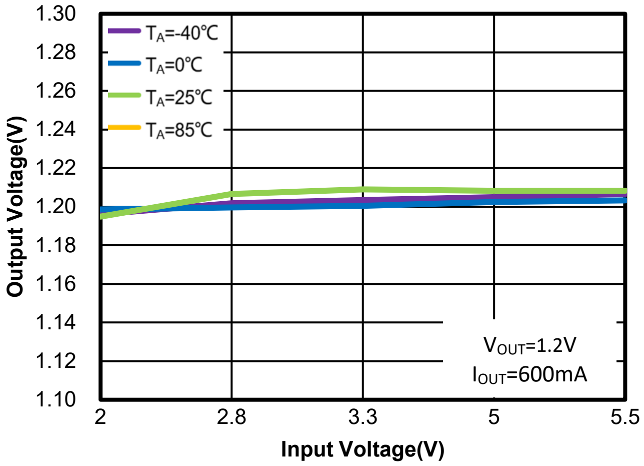


Figure19.WR0603-ADA50R
Output Voltage vs VIN & Ambient Temperature

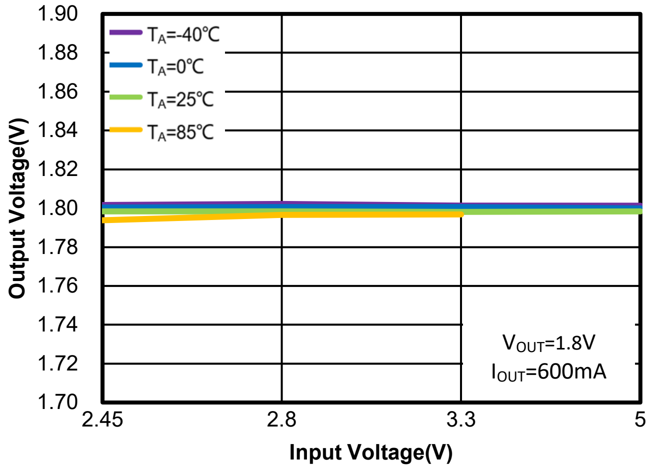


Figure20.WR0603-ADA50R
Output Voltage vs VIN & Ambient Temperature

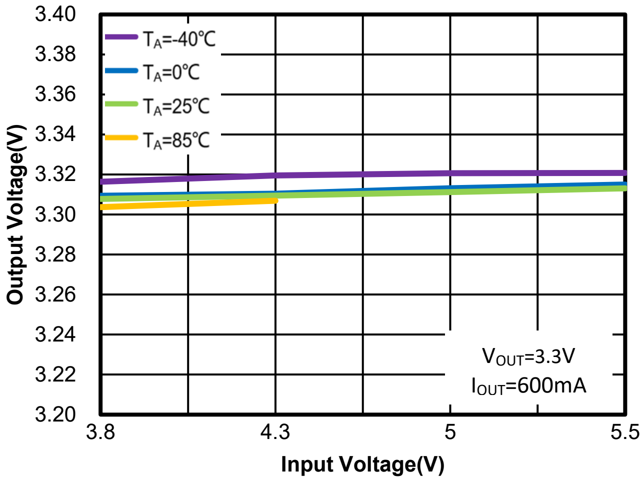


Figure21.WR0603-ADA50R
Output Voltage vs VIN & Ambient Temperature

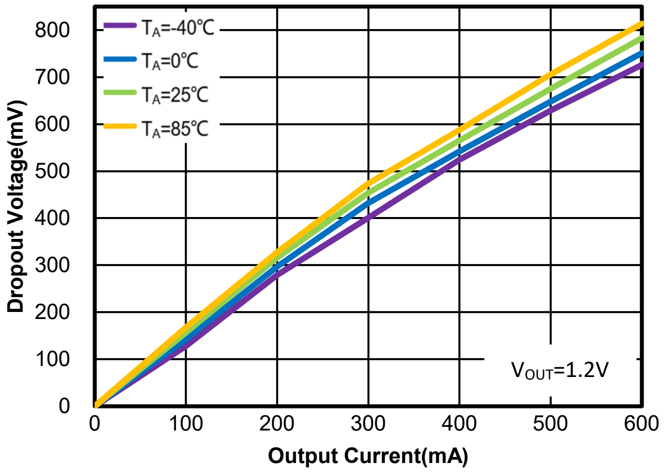


Figure22.WR0603-ADA50R
Dropout Voltage vs IOUT & Ambient Temperature

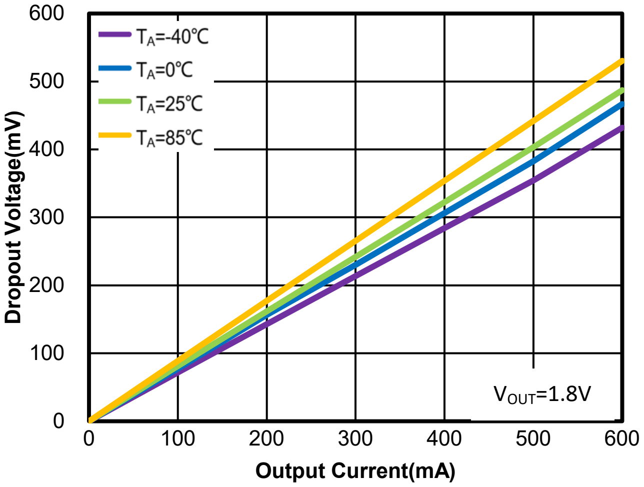


Figure23.WR0603-ADA50R
Dropout Voltage vs IOUT & Ambient Temperature

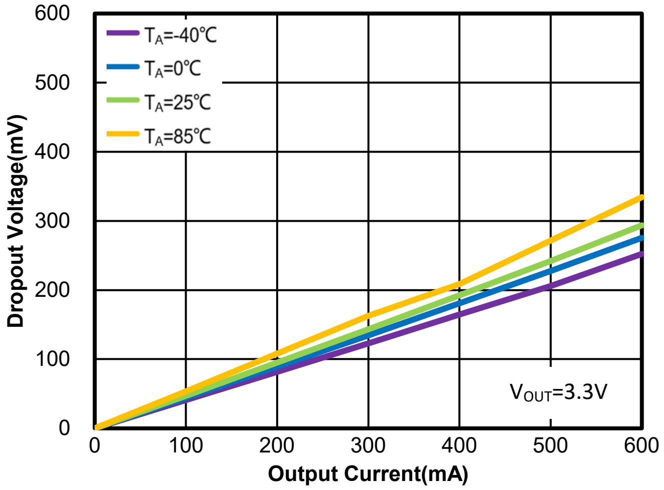


Figure24.WR0603-ADA50R
Dropout Voltage vs IOUT & Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85ºC, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

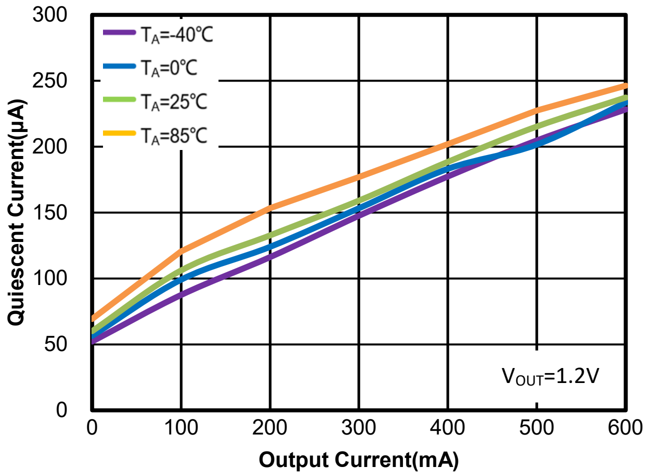


Figure 25. WR0603-ADA50R
Ground Pin Current vs. I_{OUT} & Ambient Temperature

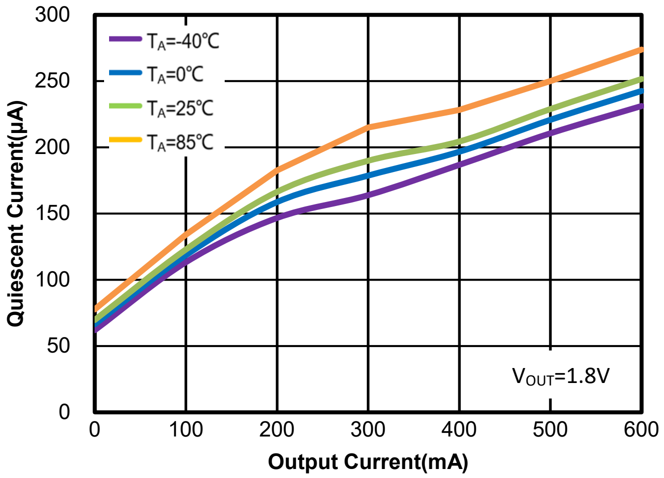


Figure 26.WR0603-ADA50R
Ground Pin Current vs. I_{OUT} & Ambient Temperature

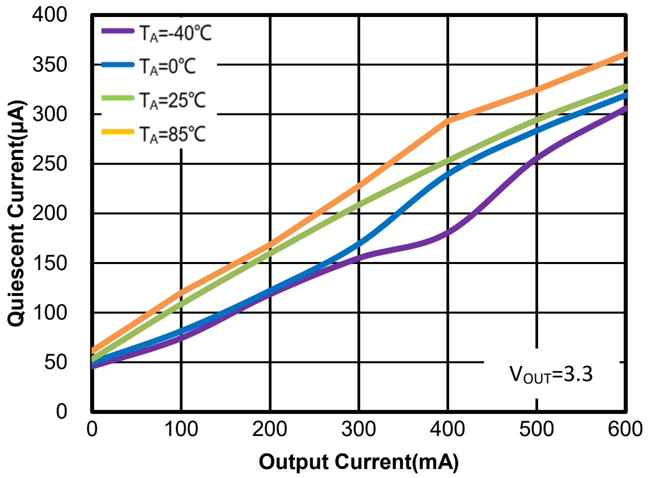


Figure 27. WR0603-ADA50R
Ground Pin Current vs. I_{OUT} & Ambient Temperature

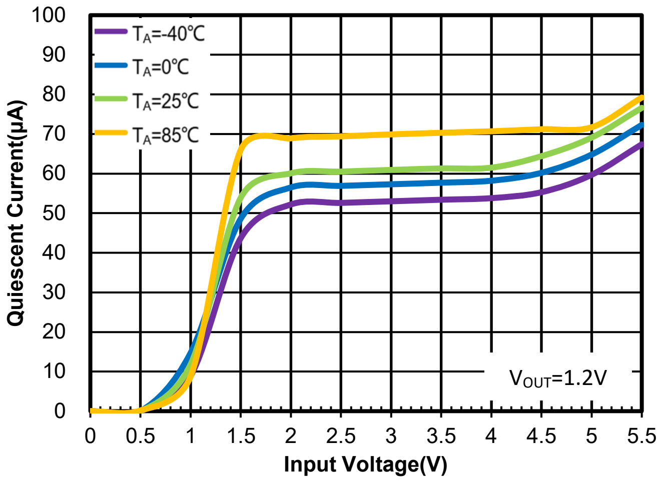


Figure 28. WR0603-ADA50R
Ground Pin Current vs. I_{OUT} & Ambient Temperature

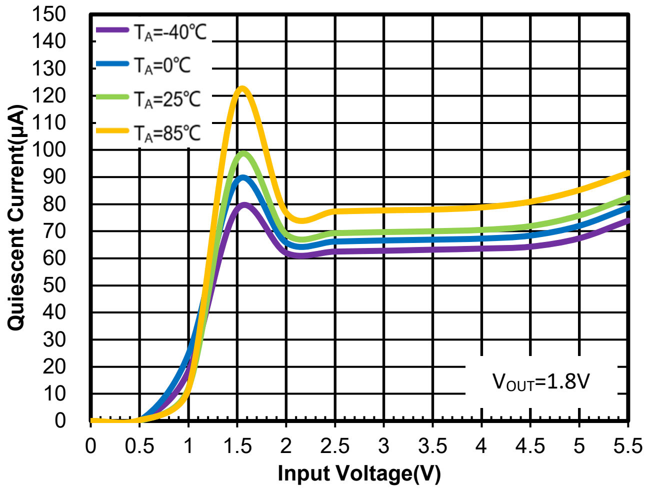


Figure 29. WR0603-ADA50R
Quiescent Current vs. V_{IN} & Ambient Temperature

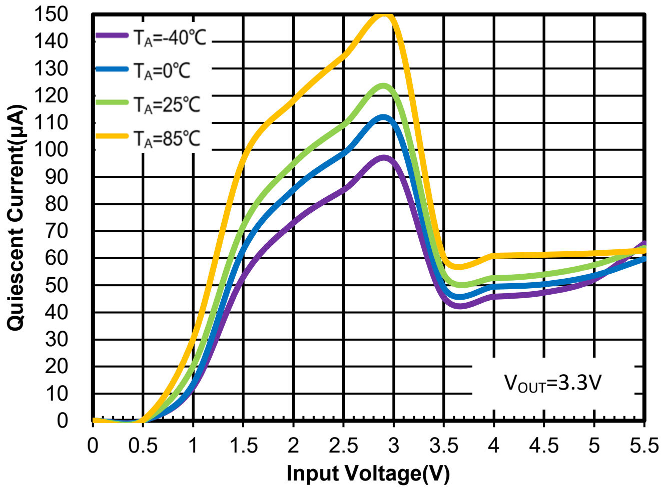


Figure 30. WR0603-ADA50R
Quiescent Current vs. V_{IN} & Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85ºC, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

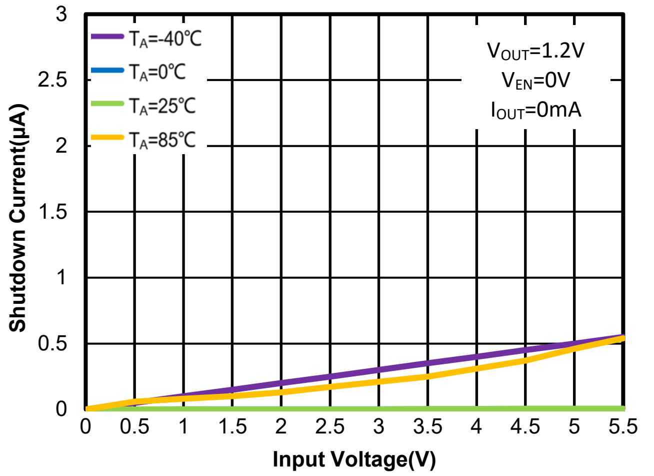


Figure 31. WR0603-ADA50R
Shutdown Current vs V_{IN} & Ambient Temperature

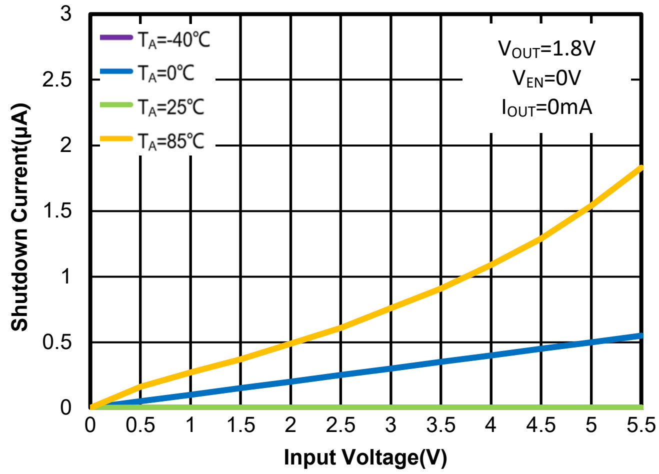


Figure 32. WR0603-ADA50R
Shutdown Current vs V_{IN} & Ambient Temperature

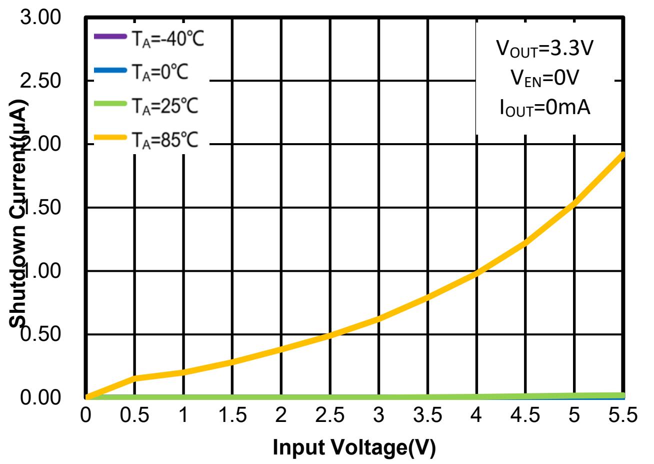


Figure 33. WR0603-ADA50R
Shutdown Current vs V_{IN} & Ambient Temperature

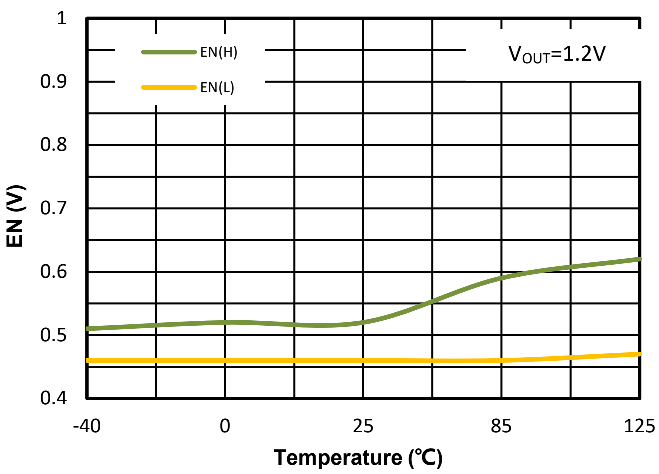


Figure 34. WR0603-ADA50R
Enable Threshold vs Ambient Temperature

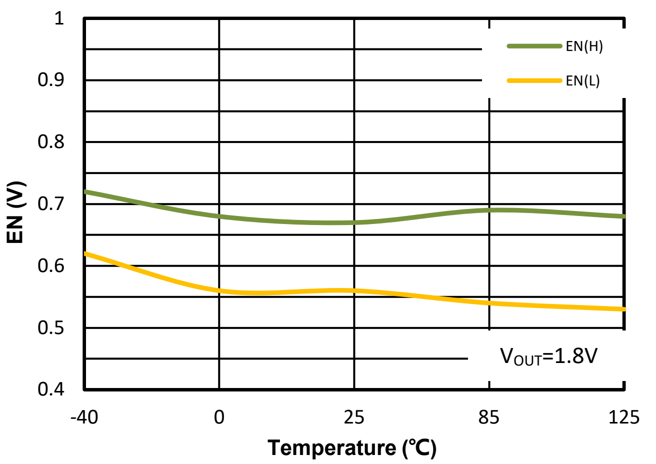


Figure 35. WR0603-ADA50R
Enable Threshold vs Ambient Temperature

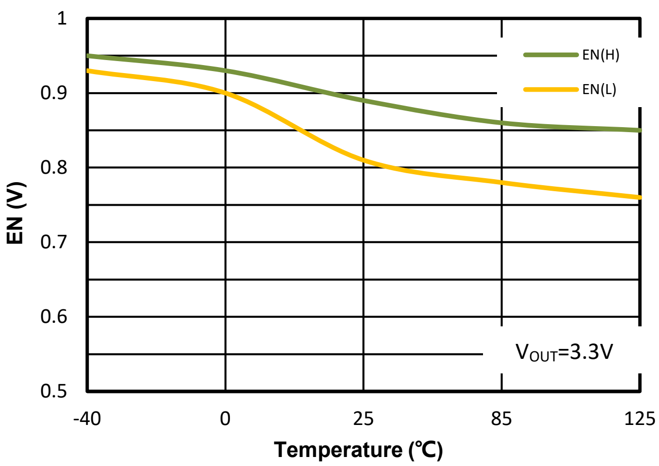


Figure 36. WR0603-ADA50R
Enable Threshold vs Ambient Temperature

Typical Performance Characteristics (TA= -40 to 85ºC, VIN=VOUT+0.5V or 2.0V,whichever is greater, CIN=COUT=1μF, unless otherwise noted)

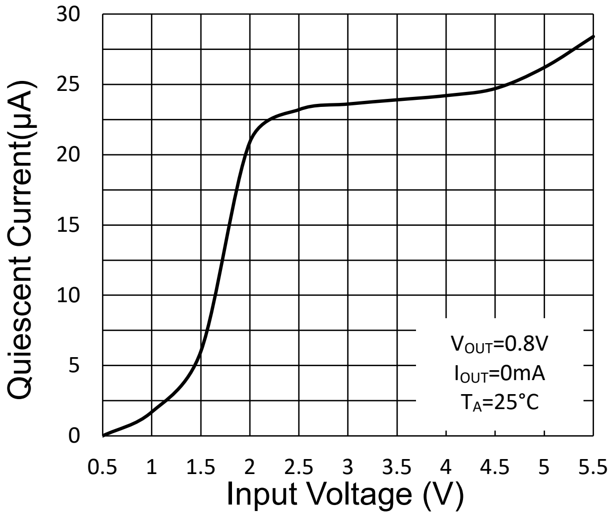


Figure 37.WR0603-ADA50R
Quiescent Current vs Supply Voltage

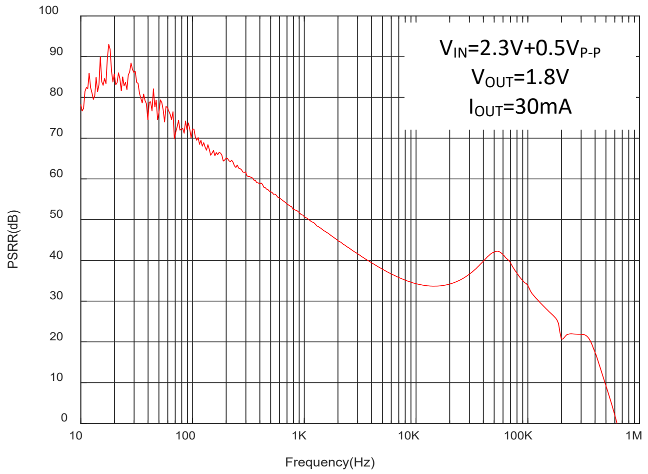


Figure 38.WR0603-ADA50R
Enable Threshold vs. Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85ºC, V_{IN}=V_{OUT}+0.5V or 2.0V,whichever is greater, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

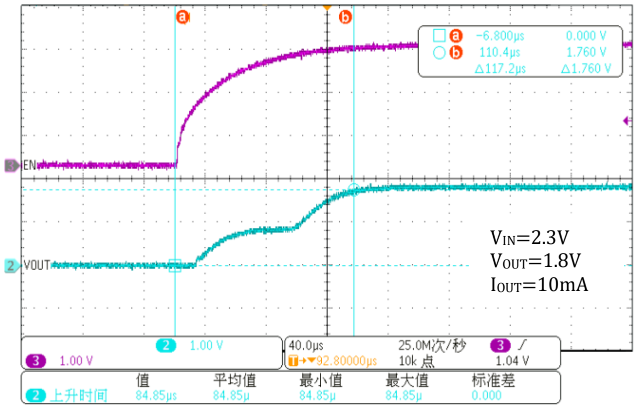


Figure 39.Soft Start from EN

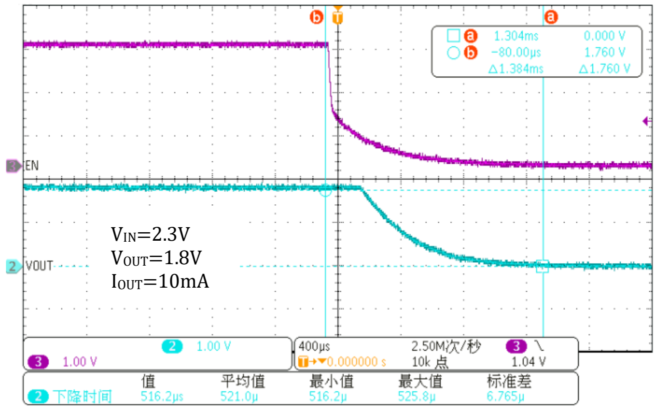


Figure 40.EN Shutdown

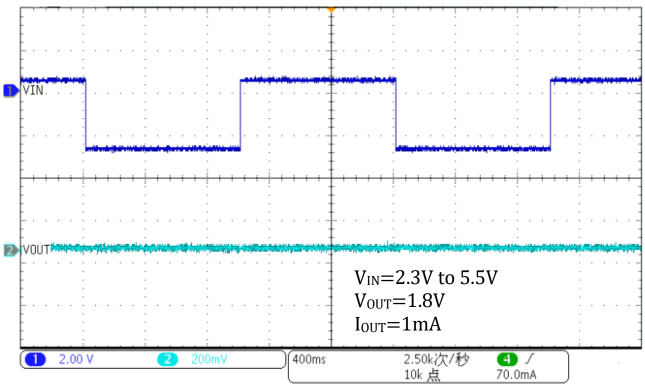


Figure 41.Line Transient

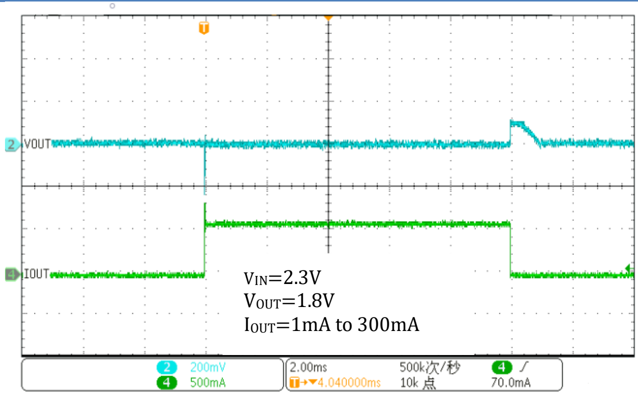


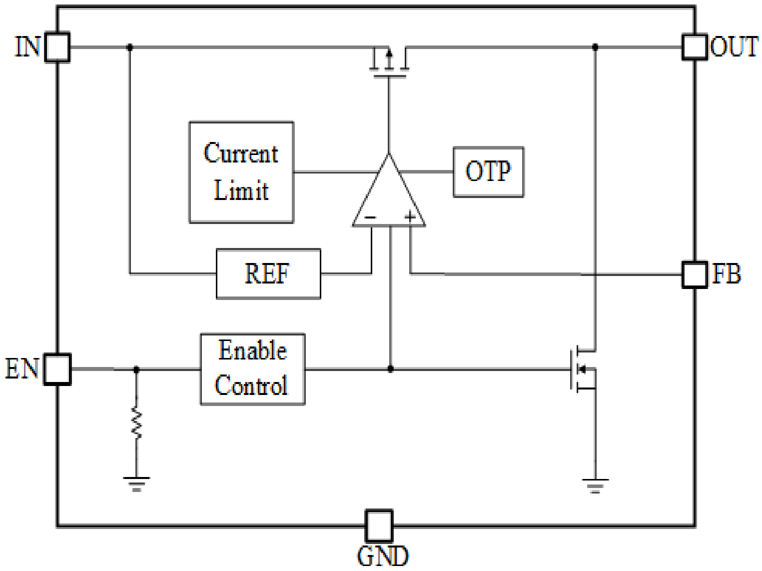
Figure 42.Load Transient

11. Function Description

11.1 Overview

The WR0603 is high performance regulator capable of supplying 600 mA and adjustable output voltage range 0.8V to 5.0V. The device also offers low quiescent current, low-dropout voltage and very small packages suitable for space constrains application. The WR0603 is designed to be used in a variety of applications.

11.2 Block Diagram



11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR0603 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Enable (EN)

When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device shutdown. If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 Dropout Voltage (V_{DO})

WR0603 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the V_{IN}-V_{OUT} at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For

CMOS regulators, the dropout voltage is determined by the $R_{DS\,(ON)}$ of the pass-FET.
The $R_{DS\,(ON)}$ is calculated as follows:

$$R_{DS\,(ON)}=V_{DO}/I_{RATED}$$

11.3.4 Power Supply Rejection Ratio(PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$\mathbf{PSRR = 20log(Ripple(in) / Ripple(out))}$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

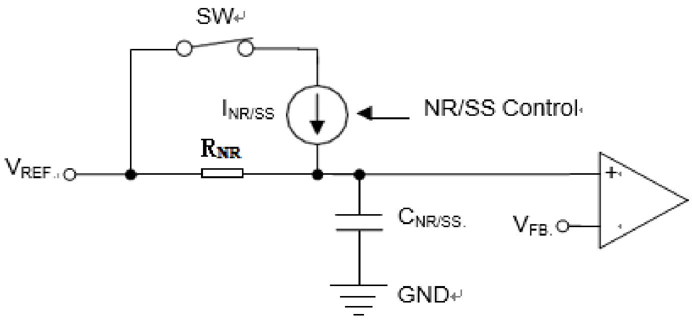
11.3.5 Noise

LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimising noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

11.3.6 Output Soft-Start

Soft-start is the ramping characteristic of the output voltage during the LDO turn-on period after EN and UVLO have exceeded the threshold, preventing the damage caused by output voltage overshoot to the subordinate circuits and enabling effective protection of the secondary circuits. The soft-start ramp can be programmed using a noise reduction capacitor. A larger value of noise reduction capacitor will reduce noise, but will also result in a slower output turn-on ramp. Higher currents allow a reasonable start-up time to be maintained with a larger noise reduction capacitor.



Soft-Start Circuit

11.3.7 Foldback Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{MAX}, and the output voltage will be reduced to $I_{MAX}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX}. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to $I_{FB}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR0603 uses a foldback current limiting mode where the final current is clamped to around 350mA, thus providing good protection to the device.

More information on current limiting can be found in Electrical Characteristics *Figure 4* to *Figure 6*.

11.3.8 Thermal Protection

The WR0603 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 140°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 125°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0603's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0603 into a thermal shutdown state will reduce the reliability of the device.

For reliable operation, limit the junction temperature to a maximum of 85°C. The thermal margin in a given layout is to be estimated. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition of the application.

11.4 Functional Mode Of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V > V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{UVLO} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(nom)}$ + V_{DO}) and is less than 5.5V.

2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.

3. The output current is less than the current limit ($I_{OUT} < I_{CL}$).

4. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

11.4.3 Disabled

The WR0603 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.4V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0603 is a linear voltage regulator with an input voltage of 2.0 V to 5.5 V and an output voltage of 0.8 V to 5.0V. The accuracy is 2% for ambient temperature 25℃ and 2.5% for ambient temperature -40℃ to 85℃. The maximum output current is 600 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Start-Up

12.1.1.1. Enable(EN)

The WR0603 can determine the output of the device through the EN input voltage, EN is higher than the voltage threshold to turn on, in order to prevent the device from turning off when the input voltage drops during the turn-on period, EN has a certain hysteresis. when EN floats default to low, if you do not need EN independent control, it is recommended to connect EN directly to IN. If you want to use the EN control, you need to give a control voltage to the EN side.

12.1.1.2. Automatic Discharge

The WR0603 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.1.3. Soft-Start

Soft start refers to the characteristic that the output voltage rises gradually as the EN voltage jumps from low to high. Reducing the output voltage rise rate reduces the inrush current that charges the output capacitor. The inrush current is the current entering the LDO during startup and consists of the load current, the current charging the output capacitor, and the ground pin current.

The inrush current can be estimated by the following equation :

$$I_{OUT}(t) = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right)$$

The WR0603 controls soft-start through an external capacitor (CNR/SS), which helps to reduce inrush current and reduce load transients on the input power bus, thus solving startup initialization problems that can result when powering FPGAs, DSPs, or other high-current loads.

12.1.2 Capacitor Recommendation

The WR0603 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good capacitance stability at different temperatures. WR0603 is designed to use ceramic capacitors of 1 µF or larger at the input and output. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device.

Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation(PD)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

PD can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators Ψ_{JT} or Ψ_{JB} are given in the thermal information table and can be used according to the following equation.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \times P_D$

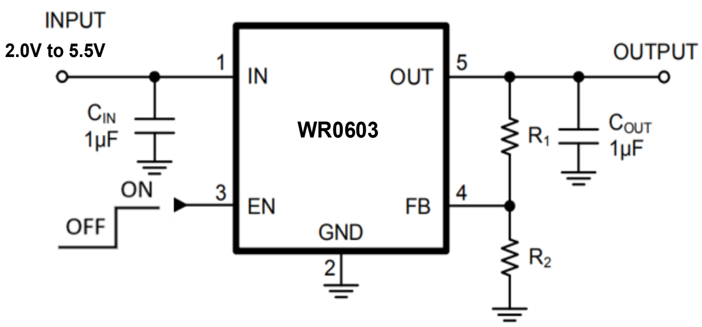
Ψ_{JB}: $T_J = T_B + \Psi_{JB} \times P_D$

Notes.

- P_D is the power dissipated.
- T_T is the temperature at the top center of the device package.
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.
-

12.1.5 Adjustable Device Feedback Resistors

The device requires external feedback divider resistors to set the output voltage.The following figure shows how the output voltage of an adjustable device can be configured from 0.8 V to 5.5 V by using a resistor divider network.



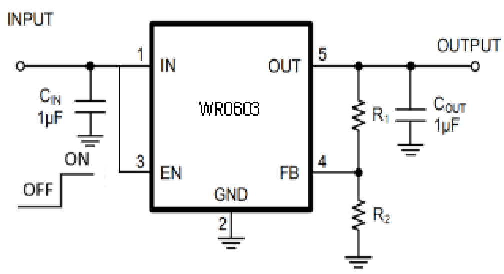
calculates the values of the R1 and R2 resistors to set the output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$$

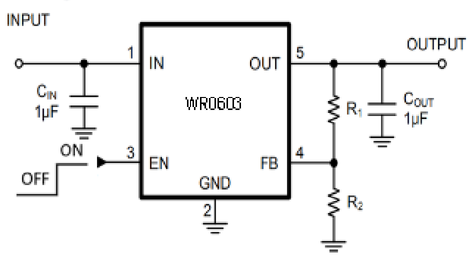
12.2 Typical Application

This section discusses the application of the WR0603 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic 1: V_{OUT} normally open, no control.



Circuit schematic 2: V_{OUT} control by external voltage to EN.



C_{IN} and C_{OUT} are to be selected with the recommended appropriate capacitance. 1µF ceramic capacitors are selected for both C_{IN} and C_{OUT} to help balance the charge needed to charge the output capacitor during startup, thus reducing the input voltage drop.

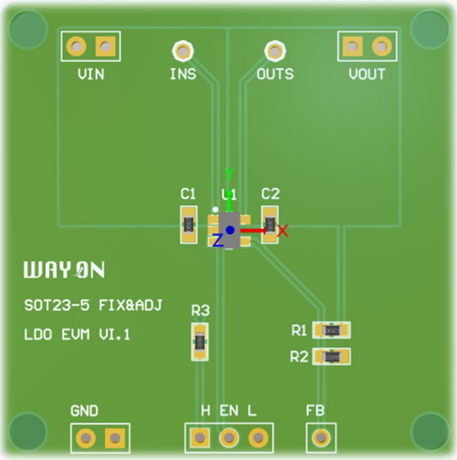
13. Power supply recommendation

The WR0603 has a V_{IN} range of between 2.0 V and 5.5 V and an input capacitance of 1μF. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.
To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

Layout Example:



15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
WR0603	SOT23-5	WAYON LDO EVM V1.1 -SOT23-5
	DFN-6	WAYON LDO EVM V1.0 -DFN2×2-6

16. Naming conventions

WR AA BB-CC DDD E

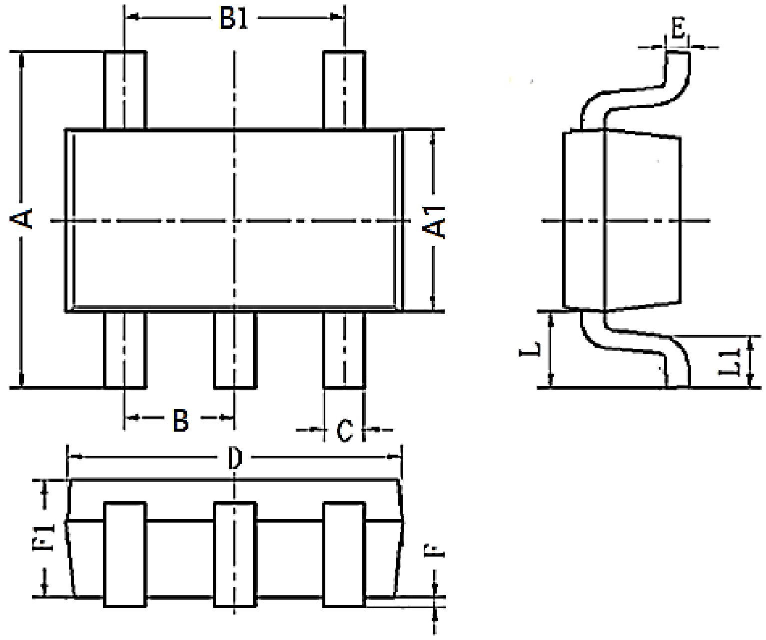
WR: WAYON Regulator
AA: 01/03/05/06 - Output Current, 100/300/500/600mA
BB: Serial number
CC: Output Voltage/AD-Output Voltage, Adjustable Voltage
DDD: A50-Package, SOT23-5
FF6- Package, DFN-6
E: R-Reel & T-tube

17. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more *susceptible* to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

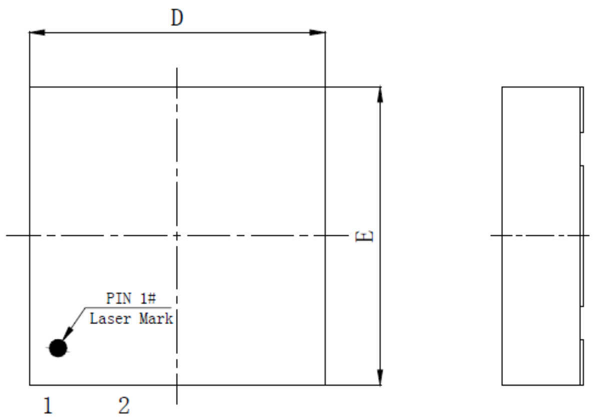
18. Package Information

SOT 23-5

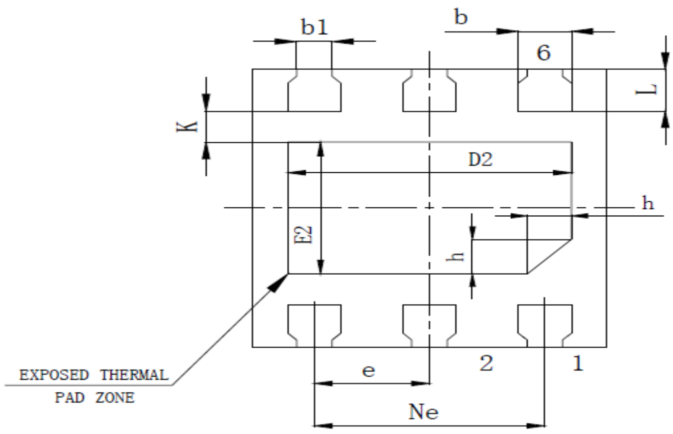


SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	2.60	2.80	3.00
A1	1.50	1.60	1.70
B	0.95BSC		
B1	1.90BSC		
C	0.25	0.40	0.50
D	2.82	2.92	3.02
E	0.10	0.15	0.20
F	0.00	0.08	0.15
L	0.59REF		
F1	0.90	1.10	1.30
L1	0.30	0.45	0.60

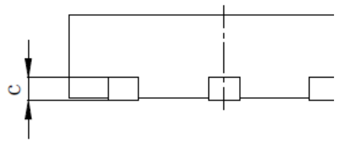
DFN-2*2-6L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.65BSC		
Ne	1.30BSC		
E	1.90	2.00	2.10
E2	0.85	0.95	1.05
L	0.25	0.30	0.35
h	0.20	0.25	0.30
K	0.20	0.225	0.28

19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0603-ADA50R	adjustable	SOT23-5	3k/Reel	WR0603 AD XXXX
WR0603-ADFF6R	adjustable	DFN2*2-6L	3k/Reel	0603 XXXX

* XXXX is variable. The chip is universal whether the marking has j or not.

STATEMENTS

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