WR0513

Ultra-Low Dropout, Input Voltage Range 5.5V, 500mA LDO

1. General Descriptions

The WR0513 series are high performance positive voltage regulators with separated bias voltage (V_{BIAS}), offering output current up to 500mA with low dropout voltage and very low quiescent current for portable applications.

The feature of ultra-low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. In addition, the WR0513 series consist of an accurate voltage-reference block, Driver block, an error amplifier, a voltage-setting resistor net, a NMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit.

The device is available in the DFN1.2X1.2-6L, DFN1.2X1.2-4L package.

2. Features

- Input Voltage Range: 0.8V to 5.5V
- Bias Voltage Range: 2.4V to 5.5V
- Output Voltage Range Fixed and Adjustable Versions: 0.6V to 3.3V(Fixed), 0.8V to 3.6V (Adjustable)
- 1.5% Output Voltage Accuracy @25ºC
- Ultra-Low Dropout: 140mV@ 500 mA
- 45μA in Operating Mode
- 0.8μA in Disable Mode
- Enable Control
- Output Active Discharge Function(optional)
- Thermal Shutdown Protection: 170ºC

3. Applications

- Battery Powered Systems
- Portable Electronic Device
- Digital Set Top Boxes

4. Typical Application

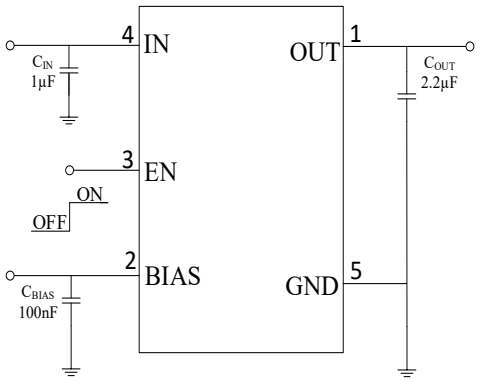
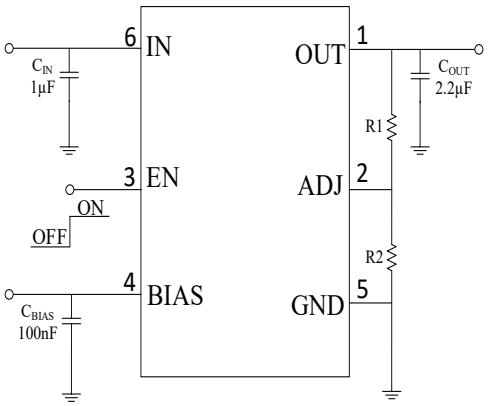


Figure 1 Fixed Voltage Regulator

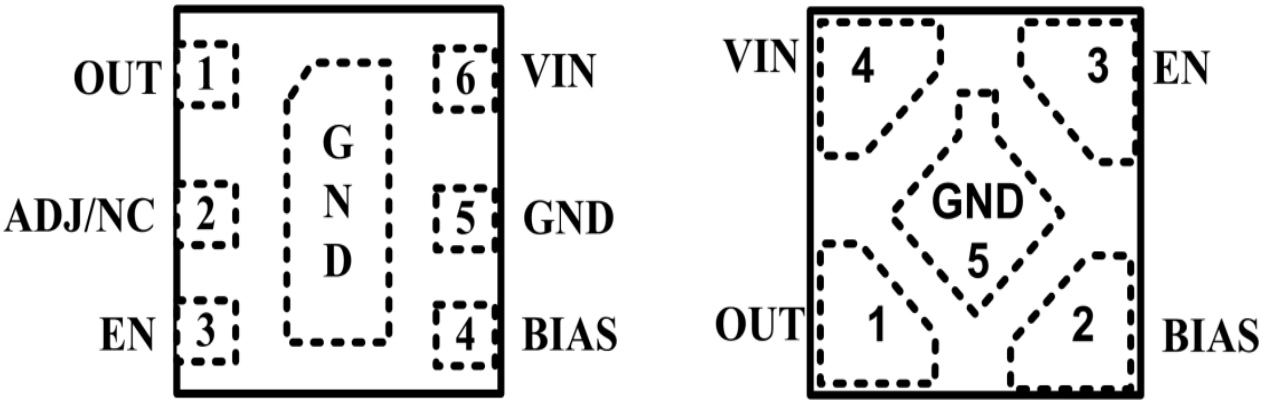


$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure 2 Adjustable Voltage Regulator

5. Pin Configuration

(Top View)



DFN1212-6L **DFN1212-4L**

6. Pin Description

PIN NUMBER		PIN NAME	PIN FUNCTIONS
DFN1212-6L	DFN1212-4L		
1	1	V_{OUT}	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 2.2μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.
2	-	ADJ/NC	ADJ: power output for the LDO NC（FIX）: Test pin internal pull down by 2μA. This pin should be floating or connected to ground.
3	3	EN	Enable input. Active High. EN includes a small pull-down current source, nominally 0.5μA.
4	2	BIAS	Supply voltage for the LDO control circuit. Mandatory to power up V_{BIAS} before EN and V_{IN}, this will ensure WR0513 performance follows datasheet spec.
5	5	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	4	V_{IN}	Input voltage supply. Bypass with a typical 1μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.

7. Absolute Maximum Ratings[1]

PARAMETER		RATING	UNIT
Input Voltage range		-0.3 to 6.0	V
EN Input voltage range		-0.3 to 6.0	
Output voltage range		-0.3 to 6.0	
Maximum output current		800	mA
Power Dissipation PD @T_A = 25ºC	DFN1.2X1.2-6L	835	mW
	DFN1.2X1.2-4L	720	
Thermal resistance[2] [4] $R_{\theta JA}$	DFN1.2X1.2-6L	149.6	℃/W
	DFN1.2X1.2-4L	173.6	
Thermal resistance[2] [3] $R_{\theta JB}$	DFN1.2X1.2-6L	130.5	
	DFN1.2X1.2-4L	137	
Top Thermal resistance[2] [3] $R_{\theta JC}$	DFN1.2X1.2-6L	50.91	
	DFN1.2X1.2-4L	53.79	
Bottom Thermal resistance[2] [3] $R_{\theta JC}$	DFN1.2X1.2-6L	28.03	
	DFN1.2X1.2-4L	30.13	
Junction Temperature		150	℃
Lead Temperature Range		260	
Storage Temperature Range		-65 to 150	
ESD Susceptibility	HBM	±4K	V

NOTE1: Greater than these given values, the device will be damaged.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 2 oz copper, no via holes on GND copper.

NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

NOTE4: Power dissipation is calculate by $P_{D(MAX)} = (T_J - T_A) / R_{\theta JA}$.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	0.8 to 5.5	V
V_{BIAS} Input voltage range	2.4 to 5.5	
EN Input voltage range	0.9 to 5.5	
Nominal output voltage range	0.6 to 3.6	
Output current range	0 to 500	mA
Input capacitor	1.0	μF
Output capacitor	2.2	
Bias capacitor	0.1	
Operating Temperature Range	-40 to 85	ºC

9. Electrical Characteristics

(V_{BIAS} = 2.4V or ($V_{OUT(NOM)}$ + 1.6V),whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{EN} = 1V, I_{OUT} = 1mA,C_{IN} = 1μF, C_{BIAS} = 0.1μF, C_{OUT} = 2.2μF, Full = -40℃ to +85℃, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage Accuracy	V_{OUT}=0.8V,no load, Full		-0.5		0.5	%
		V_{OUT}+0.3V ≤ V_{IN} ≤ V_{OUT}+1V, 1mA ≤ I_{OUT} ≤ 500mA, Full		-1.5		1.5	
V_{REF}	Reference Voltage (Adj devices only)	Full		-	0.8	-	V
V_{UVLO}	Under Voltage Lock-Out	V_{BIAS} rising, Full		-	1.6	-	V
		Hysteresis, Full		-	0.2	-	
V_{DROP_IN}	V_{IN} Dropout Voltage[1]	I_{OUT}=150mA, Full		-	37	75	mV
		I_{OUT}=500mA, Full	V_{OUT}= 0.8V	-	120	250	
			V_{OUT}= 1.05V	-	140	250	
			V_{OUT}= 1.2V	-	160	250	
			V_{OUT}= 3.3V	-	180	250	
V_{DROP_BIAS}	V_{BIAS} Dropout voltage[1]	V_{IN}= V_{BIAS} ,I_{OUT}=500mA, Full		-	1.2	1.5	V
ΔV_{LINE_IN}	V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.3V≤ V_{IN} ≤5V, Full		-	0.01	-	%/V
ΔV_{LINE_BIAS}	V_{BIAS} Line Regulation	($V_{OUT(NOM)}$ + 1.6V) ≤ V_{BIAS} ≤ 5.5V, Full		-	0.01	-	%/V
ΔV_{LOAD}	Load Regulation	I_{OUT}=1mA to 500mA, Full		-	5	-	mV
I_{LIM}	Output Current Limit	V_{OUT}= 90% $V_{OUT(NOM)}$, T_A=25℃		550	900	1200	mA
I_{OUT}	Output Current[2]	V_{OUT}= 98.5% $V_{OUT(NOM)}$, Full		500	-	-	mA
I_{SHORT}	Short Current	V_{OUT}= 0 V, T_A=25℃		-	400	-	mA
I_{ADJ}	ADJ Pin Operation Current (ADJ devices only)	T_A=25℃		-	0.1	0.5	μA
I_{BIAS}	Bias Pin Operating Current	V_{BIAS}=$V_{OUT(NOM)}$ + 1.6V, Full		-	45	80	μA
$I_{BIAS(DIS)}$	Bias Pin Shutdown Current	V_{EN} ≤ 0.4V, Full		-	0.8	1.3	μA
$I_{IN(DIS)}$	V_{IN} Pin Shutdown Current	V_{EN} ≤ 0.4V, T_A=25℃		-	0.5	1	μA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENH}	Enable Threshold Voltage	Logic _ High, Full	0.9	-	-	V
V_{ENL}		Logic _ Low, Full	-	-	0.5	V
I_{EN}	EN Pull Down Current	V_{EN}=5.5V,V_{BIAS}=5.5V,T_A=25℃	-	0.5	-	μA
t_{ON}	Turn-On Time	From assertion of V_{EN} to V_{OUT} =90% $V_{OUT(NOM)}$). $V_{OUT(NOM)}$ = 1V, T_A=25℃	-	150	-	μs
PSRR_V_{IN}	Power Supply Rejection Ratio	V_{IN} to V_{OUT} , f=1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V,T_A=25℃	-	70	-	dB
PSRR_V_{BIAS}		V_{BIAS} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V, T_A=25℃	-	65	-	dB
e_{NO_FIXED}	Output Noise Voltage (Fixed Volt.)	V_{IN}=V_{OUT}+0.5V, $V_{OUT(NOM)}$=1V, f=10Hz to 100kHz,T_A=25℃	-	40	-	μV_{RMS}
e_{NO_ADJ}	Output Noise Voltage (Ad Volt.)	V_{IN} =V_{OUT}+0.5V, f=10Hz to 100kHz,T_A=25℃	-	50* V_{OUT}	-	μV_{RMS}
T_{SD}	Thermal Shutdown Threshold	Temperature increasing	-	170	-	ºC
		Temperature decreasing	-	145	-	ºC
R_{DISCHG}	Output Discharge Pull-Down	V_{EN}<0.4V， V_{OUT}=0.5V, T_A=25℃	-	150	-	Ω

Note1: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$*97%.

Note2: Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN}< V_{OUT} + V_{DROP}.

10. Typical Performance Characteristics

(V_{BIAS} = 2.4V or ($V_{OUT(NOM)}$ + 1.6V), whichever is greater, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{EN} = 1V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{BIAS} = 0.1μF, C_{OUT} =2.2μF, Full = -40ºC to +85ºC, unless otherwise noted.)

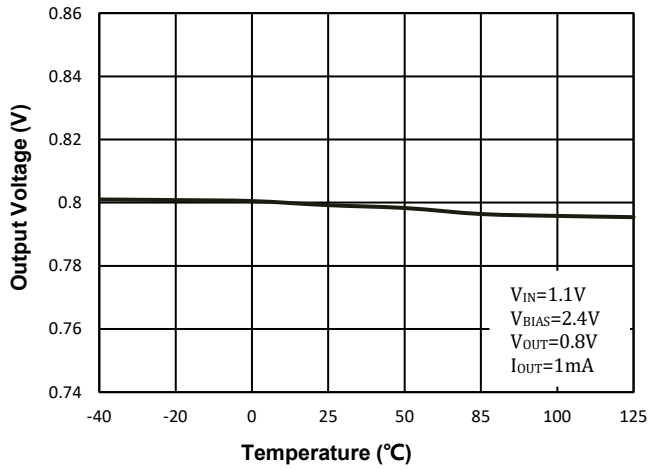


Figure 1. WR0513-ADF16R (0.8V)
Output Voltage vs. Ambient Temperature

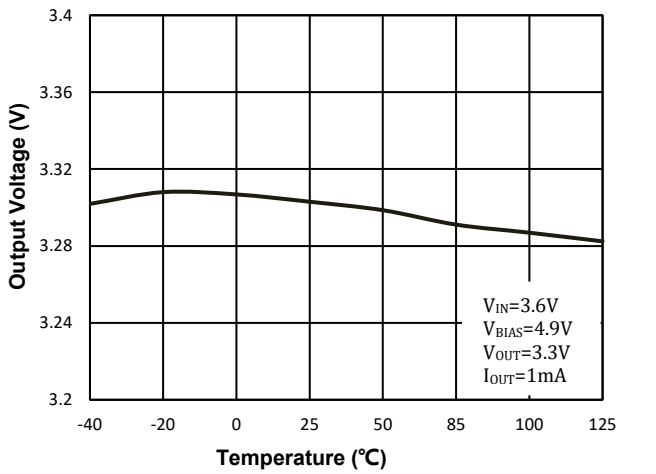


Figure 2. WR0513-ADF16R (3.3V)
Output Voltage vs. Ambient Temperature

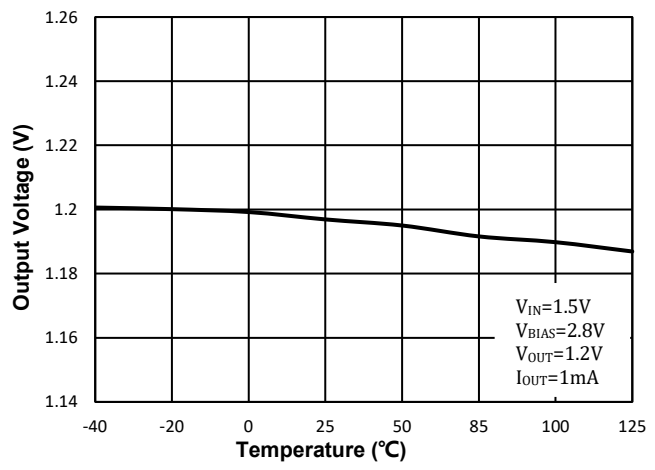


Figure 3. WR0513-12F14R
Output Voltage vs. Ambient Temperature

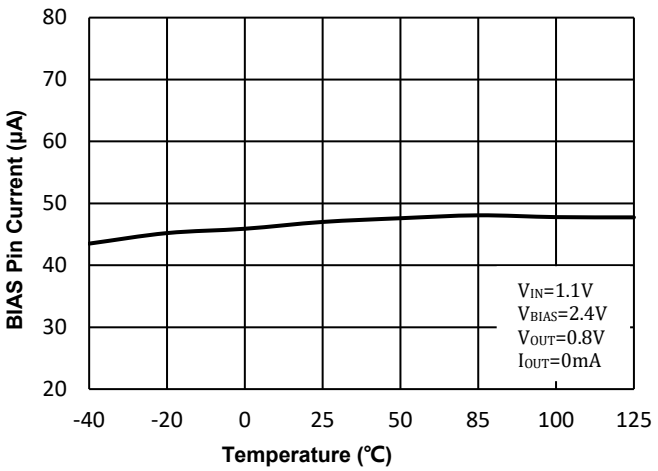


Figure 4. WR0513-ADF16R (0.8V)
Bias Pin Current vs. Ambient Temperature

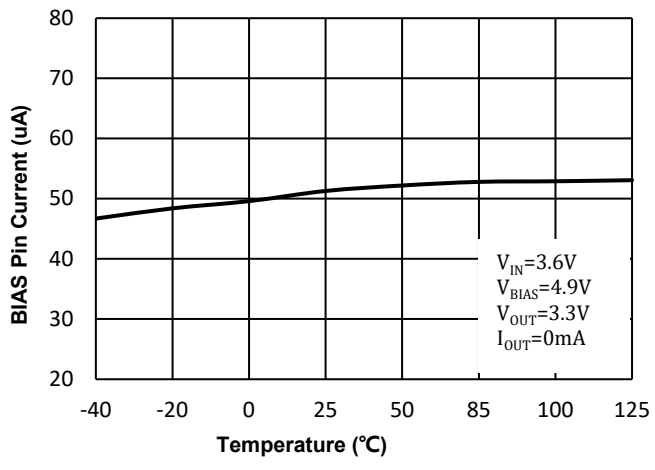


Figure 5. WR0513-ADF16R (3.3V)
Bias Pin Current vs. Ambient Temperature

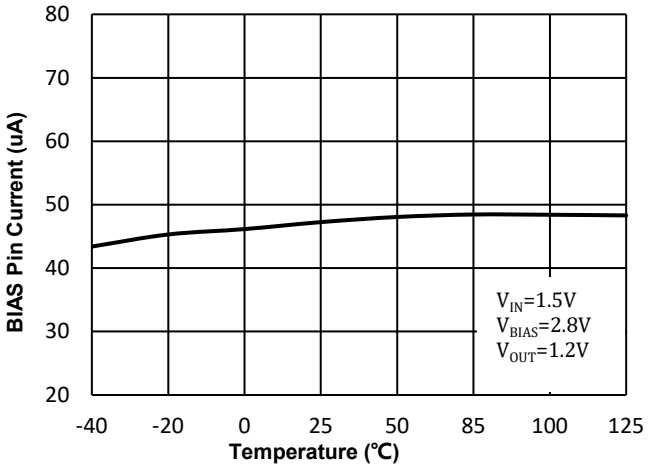


Figure 6. WR0513-12F14R
Bias Pin Current vs. Ambient Temperature

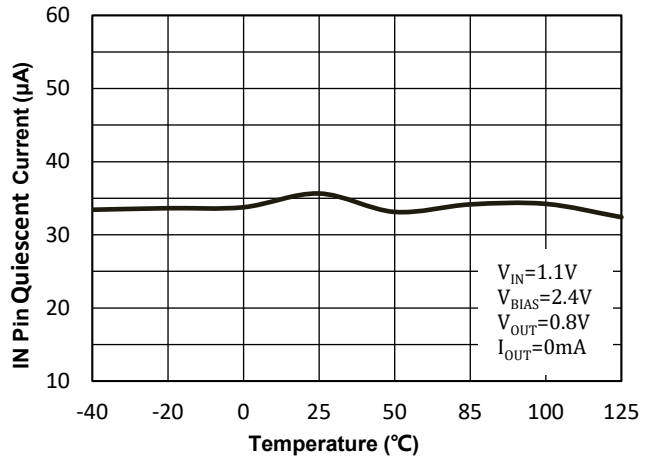


Figure 7. WR0513-ADF16R (0.8V)
IN Pin Current vs. Ambient Temperature

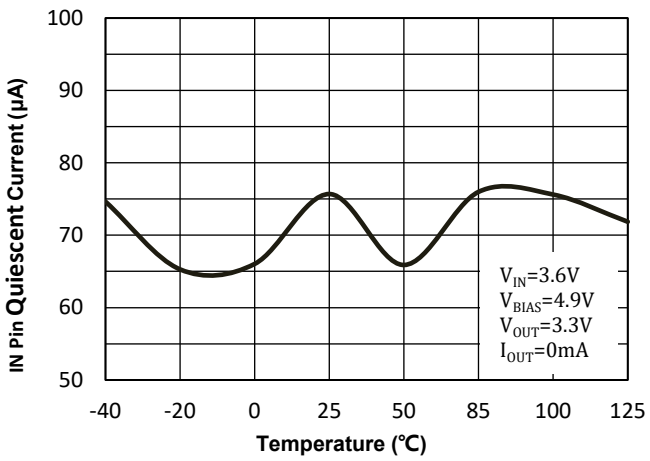


Figure 8. WR0513-ADF16R (3.3V)
IN Pin Current vs. Ambient Temperature

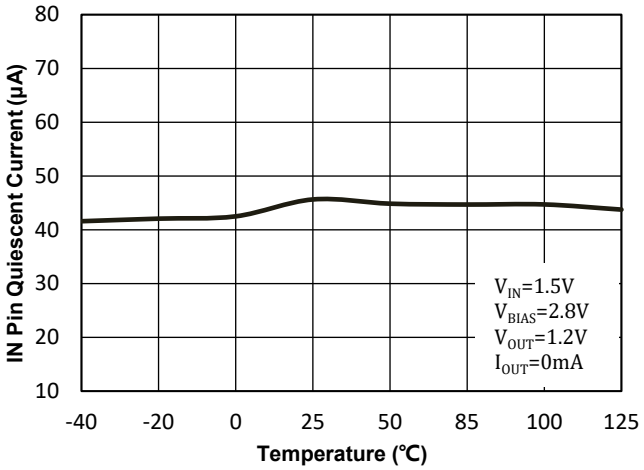


Figure 9. WR0513-12F14R
IN Pin Current vs. Ambient Temperature

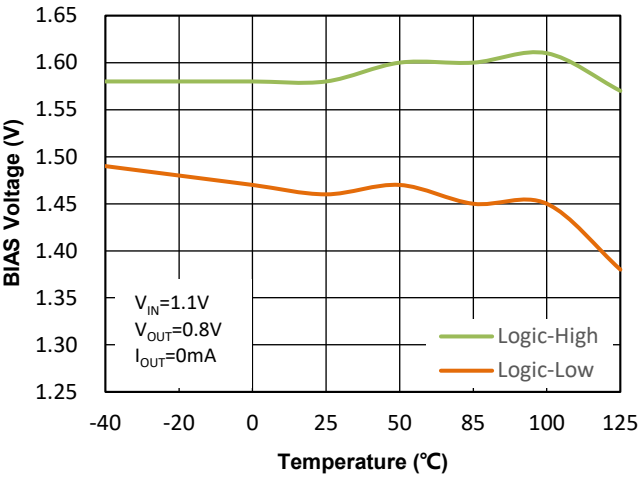


Figure 10. WR0513-ADF16R (0.8V)
BIAS Voltage UVLO vs. Ambient Temperature

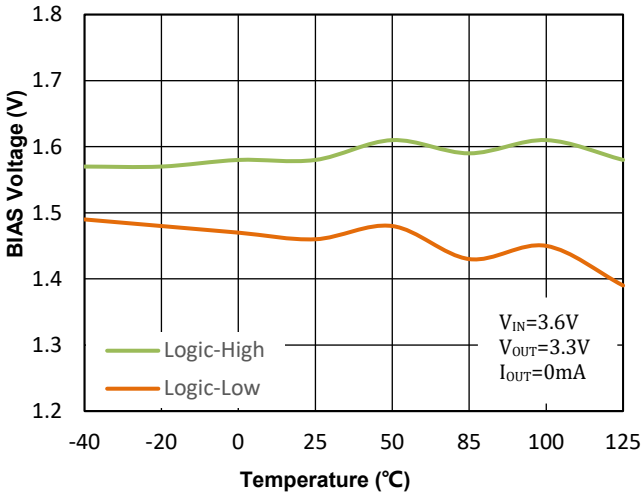


Figure 11. WR0513-ADF16R (3.3V)
BIAS Voltage UVLO vs. Ambient Temperature

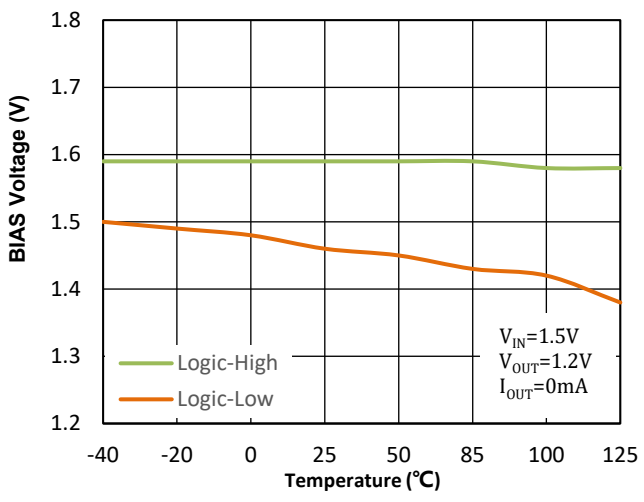


Figure 12. WR0513-12F14R
BIAS Voltage UVLO vs. Ambient Temperature

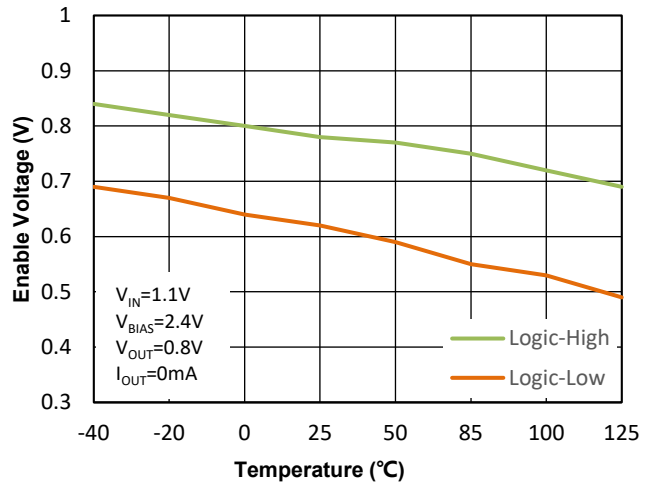


Figure 13. WR0513-ADF16R (0.8V)
Enable Voltage Threshold vs. Ambient Temperature

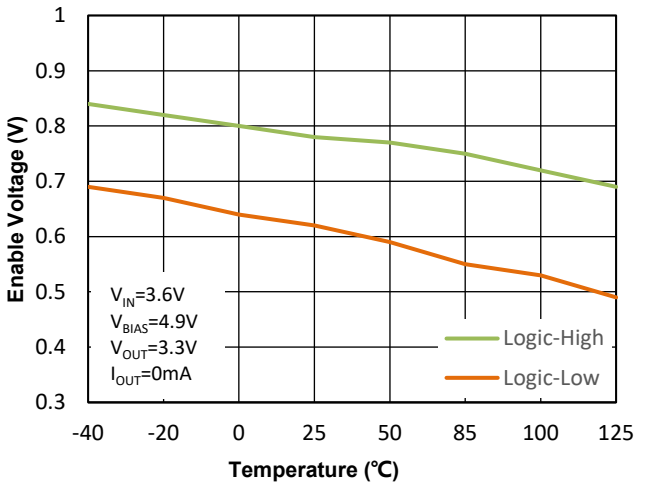


Figure 14. WR0513-ADF16R (3.3V)
Enable Voltage Threshold vs. Ambient Temperature

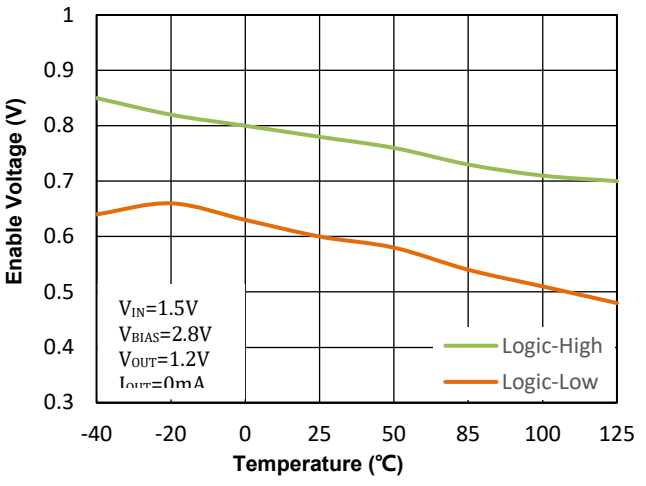


Figure 15. WR0513-12F14R
Enable Voltage Threshold vs. Ambient Temperature

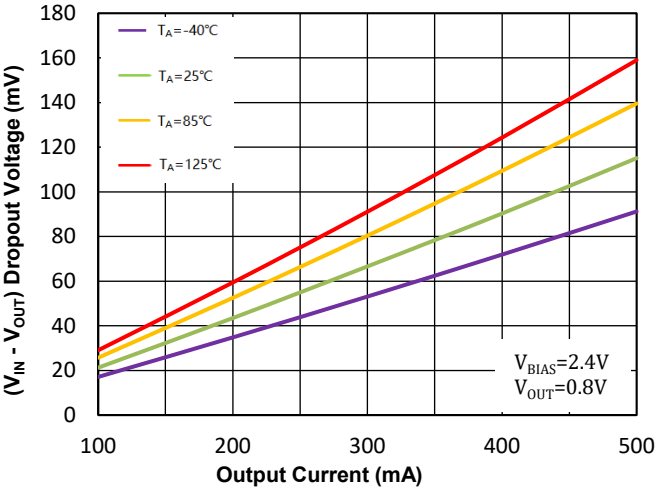


Figure 16. WR0513-ADF16R (0.8V)
Dropout Voltage _ V_{IN} vs. Ambient Temperature

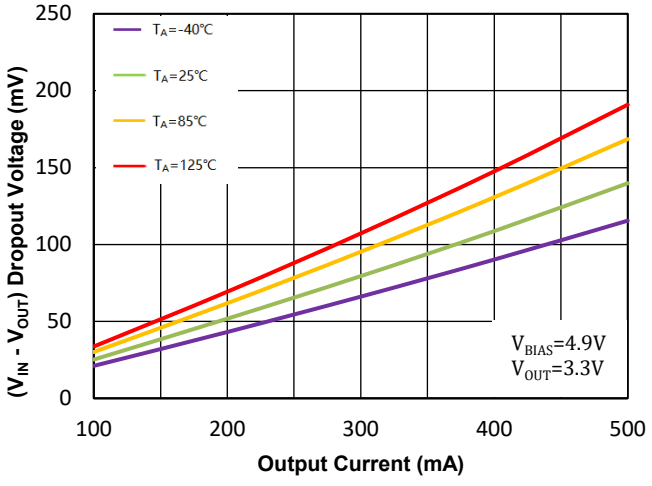


Figure 17. WR0513-ADF16R (3.3V)
Dropout Voltage _V_{IN} vs. Ambient Temperature

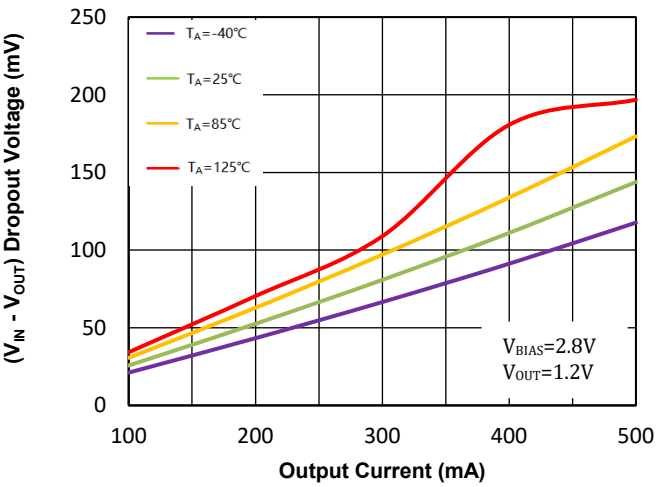


Figure 18. WR0513-12F14R
Dropout Voltage _V_{IN} vs. Ambient Temperature

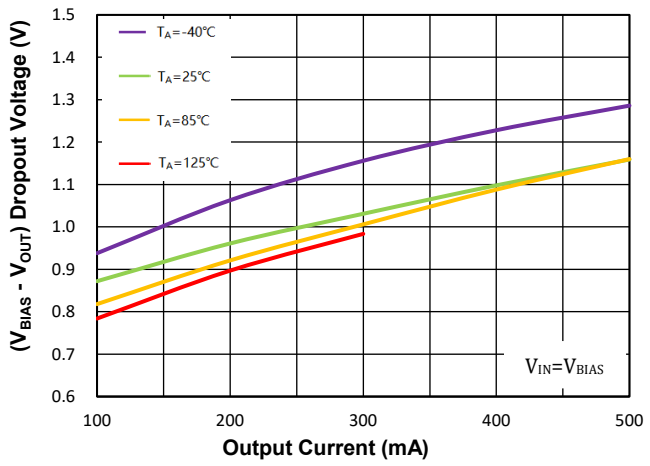


Figure 19. WR0513-ADF16R (0.8V)
Dropout Voltage _ V_{BIAS} vs. Ambient Temperature

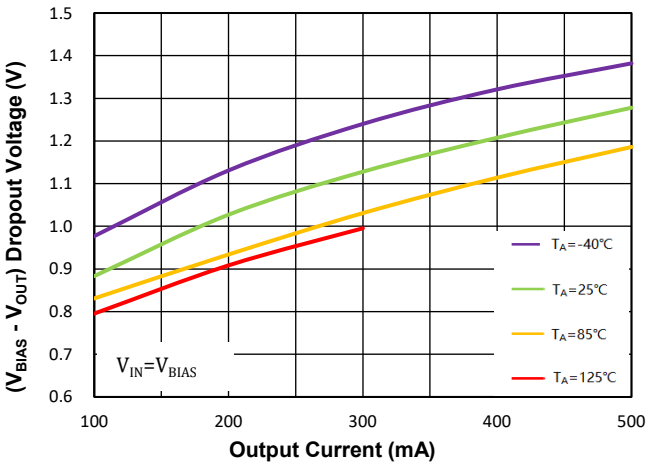


Figure 20. WR0513-ADF16R (3.3V)
Dropout Voltage _ V_{BIAS} vs. Ambient Temperature

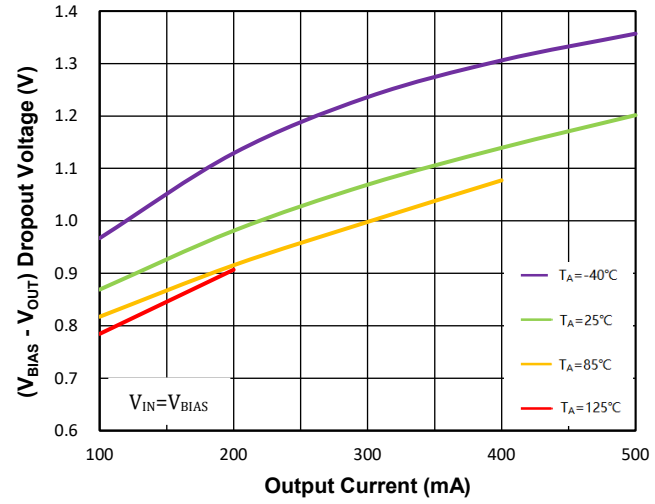


Figure 21. WR0513-12F14R
Dropout Voltage _ V_{BIAS} vs. Ambient Temperature

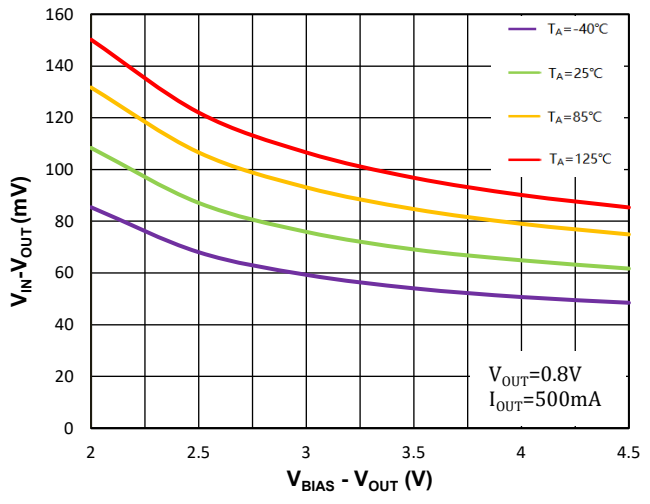


Figure 22. WR0513-ADF16R (0.8V)
V_{IN} Dropout Voltage & (V_{BIAS} - V_{OUT}) vs. Ambient Temperature

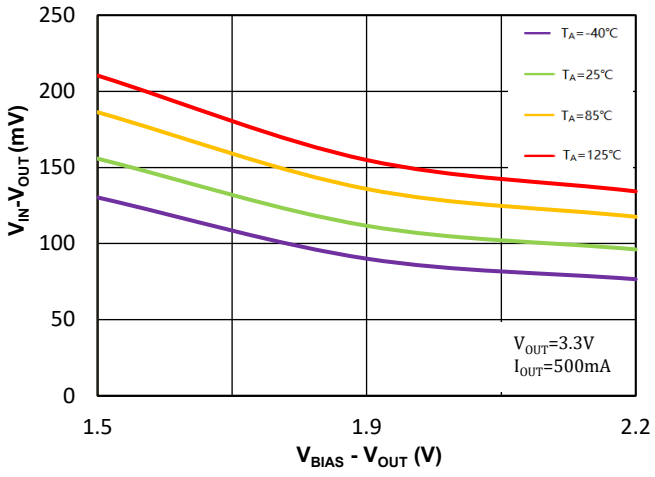


Figure 23. WR0513-ADF16R (3.3V)
V_{IN} Dropout Voltage & (V_{BIAS} - V_{OUT}) Vs. Ambient Temperature

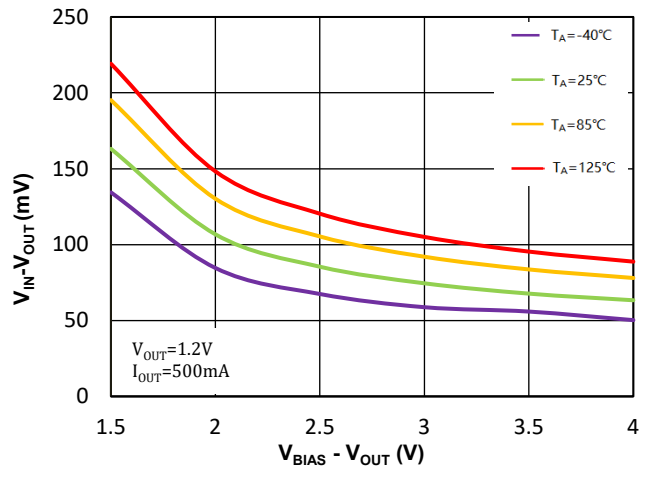


Figure 24. WR0513-12F14R
V_{IN} Dropout Voltage & (V_{BIAS} - V_{OUT}) Vs. Ambient Temperature

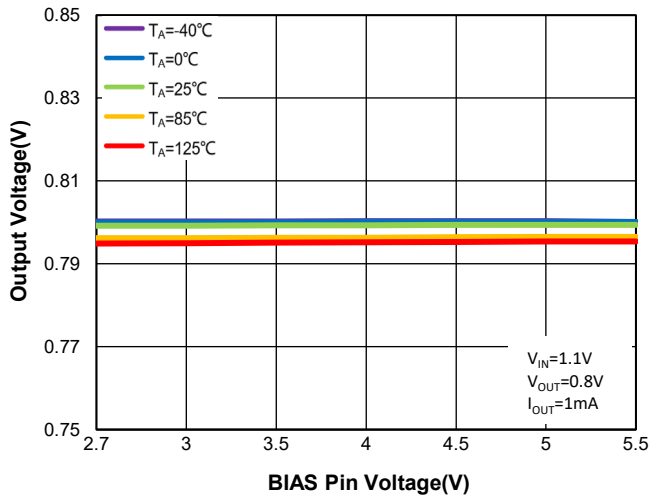


Figure 25. WR0513-ADF16R (0.8V)
Regulation vs. V_{BIAS} & Ambient Temperature

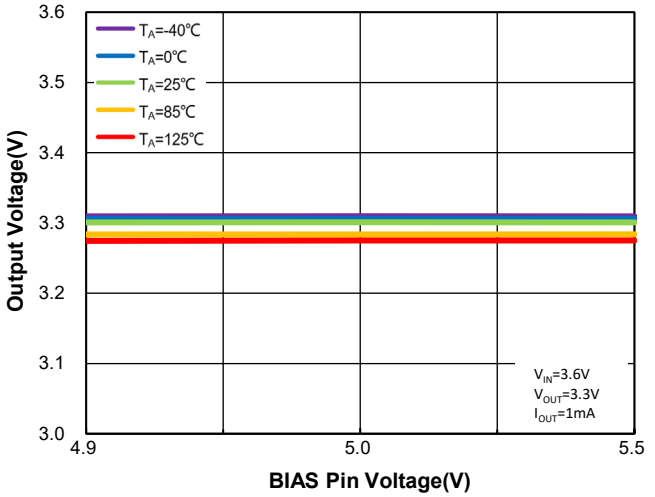


Figure 26. WR0513-ADF16R (3.3V)
Regulation vs. V_{BIAS} & Ambient Temperature

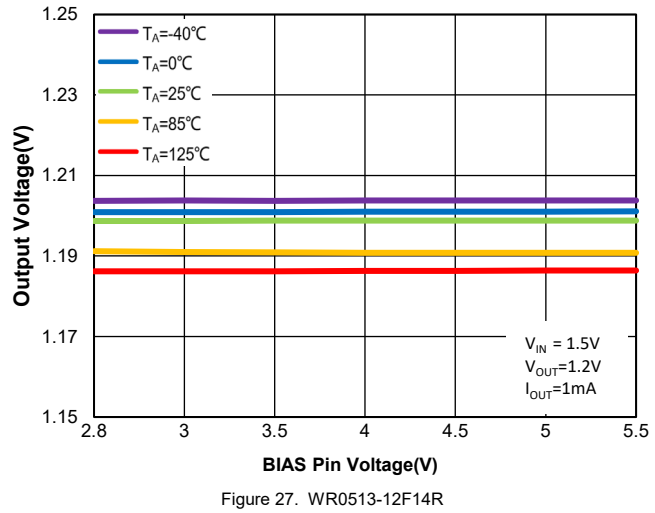


Figure 27. WR0513-12F14R
Regulation vs. V_{BIAS} & Ambient Temperature

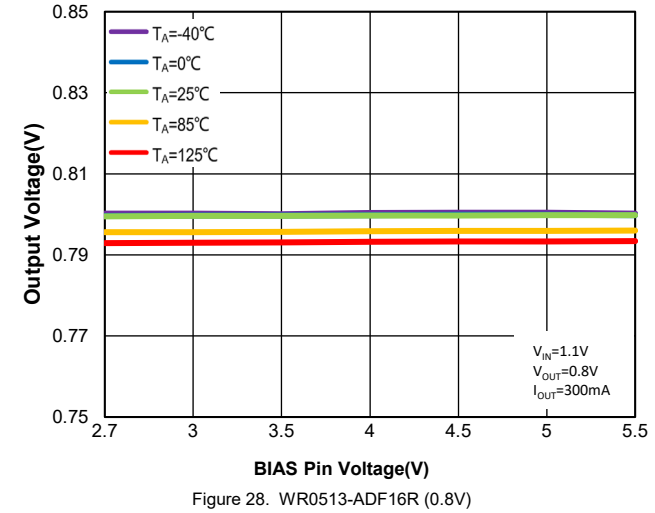


Figure 28. WR0513-ADF16R (0.8V)
Regulation vs. V_{BIAS} & Ambient Temperature

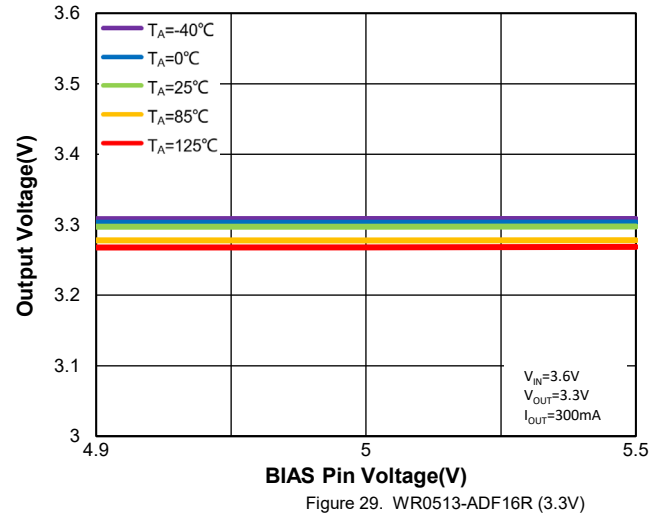


Figure 29. WR0513-ADF16R (3.3V)
Regulation vs. V_{BIAS} & Ambient Temperature

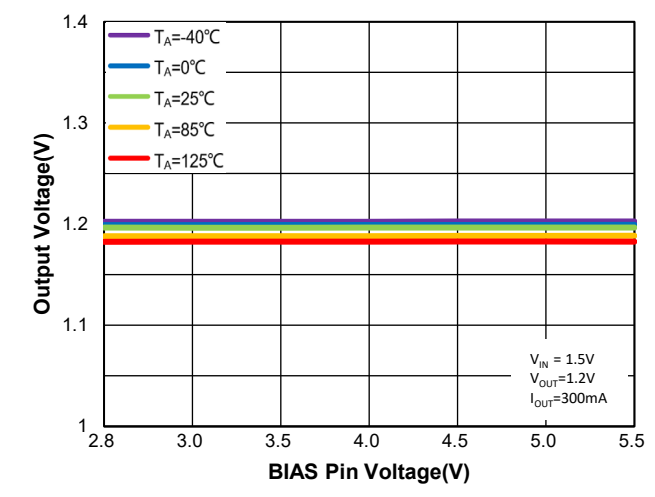


Figure 30. WR0513-12F14R
Regulation vs. V_{BIAS} & Ambient Temperature

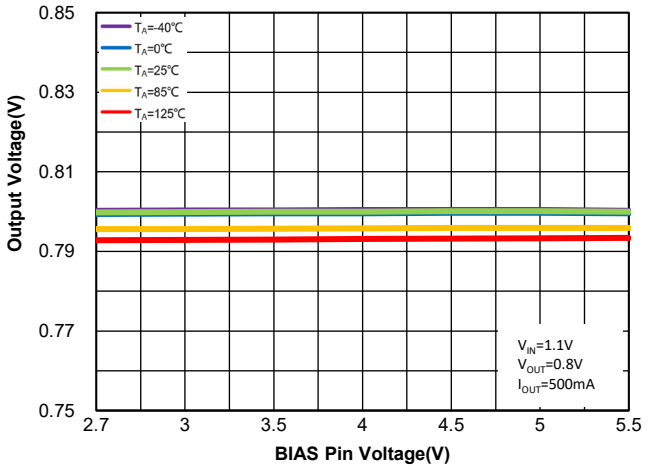


Figure 31. WR0513-ADF16R (0.8V)
Regulation vs. V_{BIAS} & Ambient Temperature

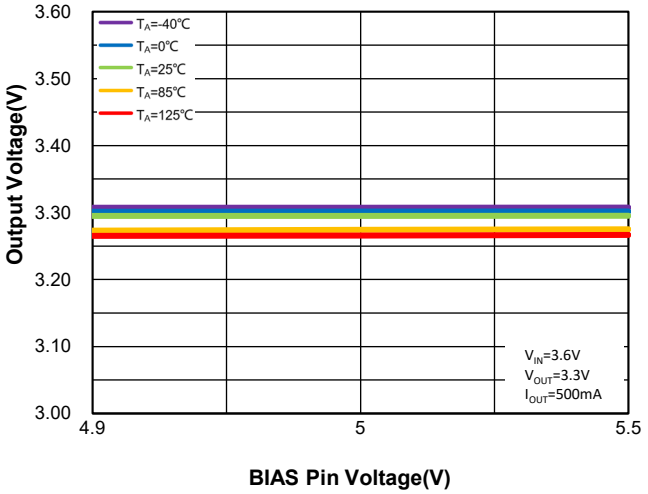


Figure 32. WR0513-ADF16R (3.3V)
Regulation vs. V_{BIAS} & Ambient Temperature

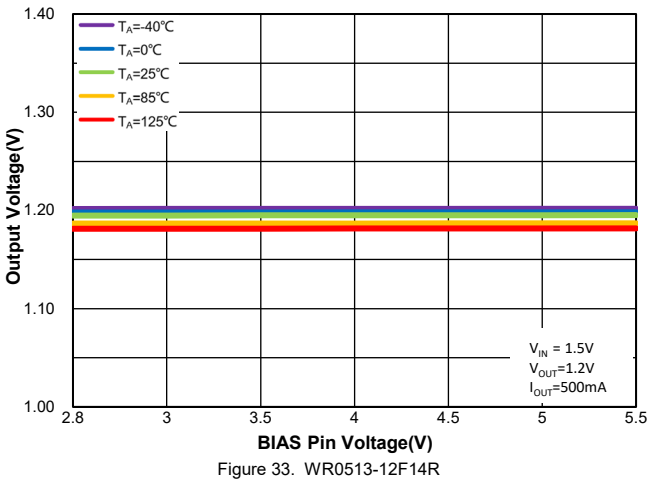


Figure 33. WR0513-12F14R
Regulation vs. V_{BIAS} & Ambient Temperature

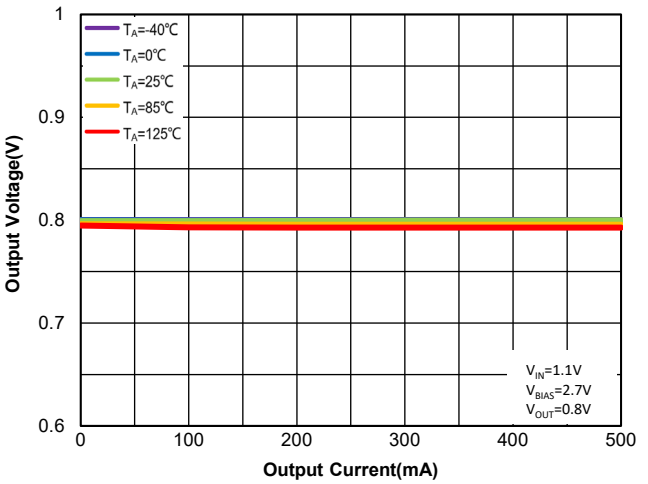


Figure 34. WR0513-ADF16R (0.8V)
Load Regulation vs. I_{OUT} & Ambient Temperature

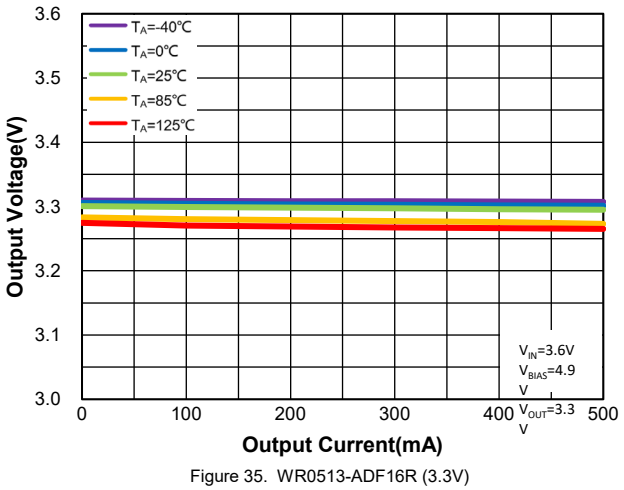


Figure 35. WR0513-ADF16R (3.3V)
Load Regulation vs. I_{OUT} & Ambient Temperature

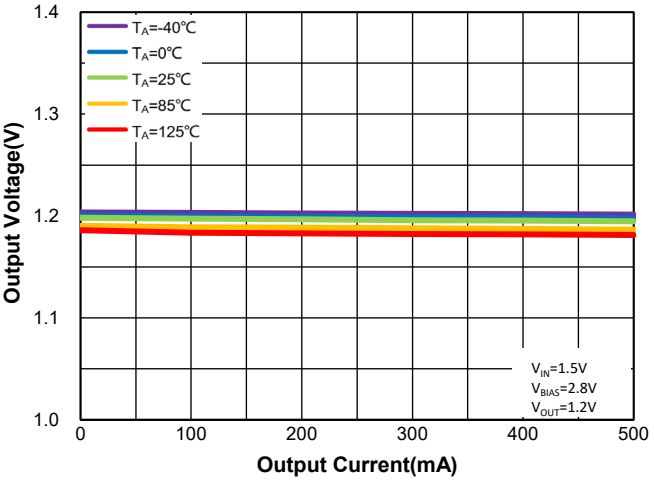


Figure 36. WR0513-12F14R
Load Regulation vs. I_{OUT} & Ambient Temperature

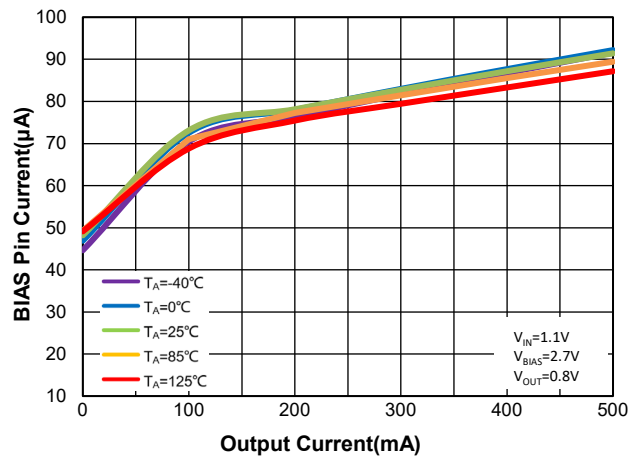


Figure 37. WR0513-ADF16R (0.8V)
BIAS Pin Current vs. I_{OUT} & Ambient Temperature

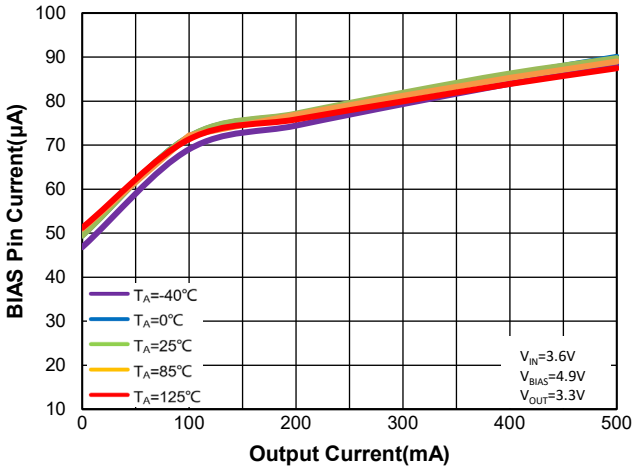


Figure 38. WR0513-ADF16R (3.3V)
BIAS Pin Current vs. I_{OUT} & Ambient Temperature

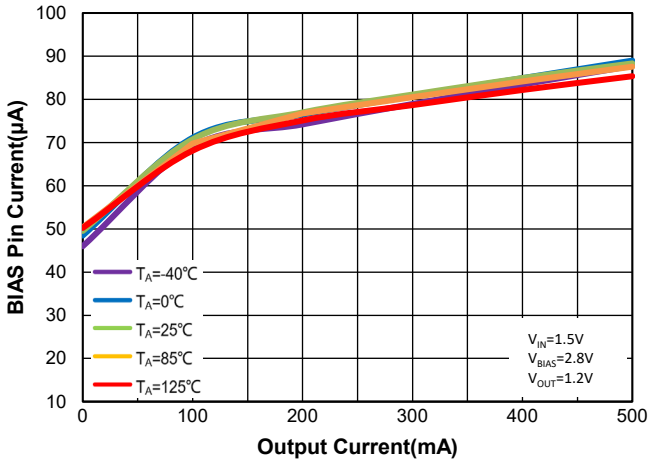


Figure 39. WR0513-12F14R
BIAS Pin Current vs. I_{OUT} & Ambient Temperature

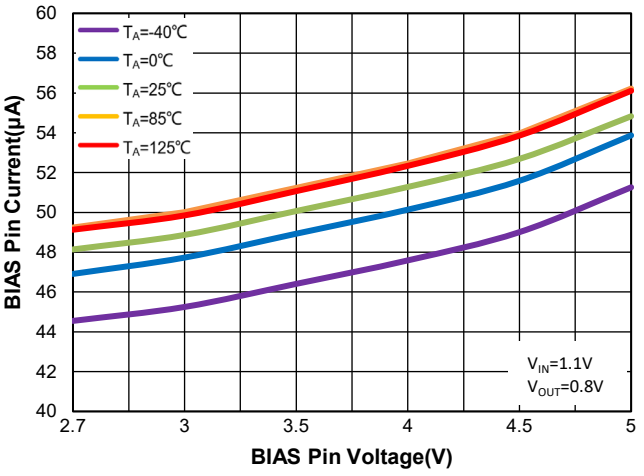


Figure 40. WR0513-ADF16R (0.8V)
BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

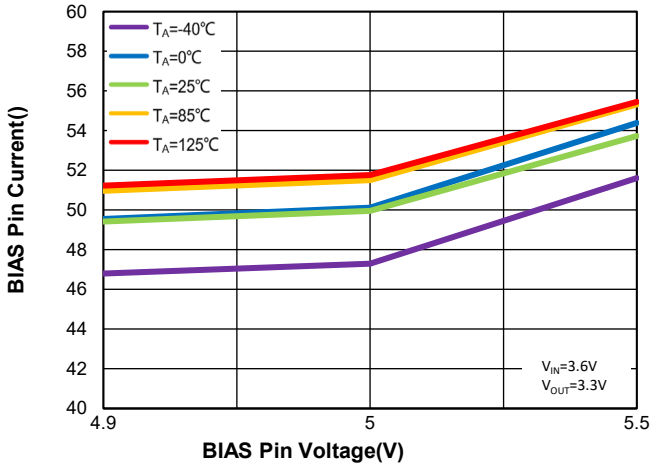


Figure 41. WR0513-ADF16R (3.3V)
BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

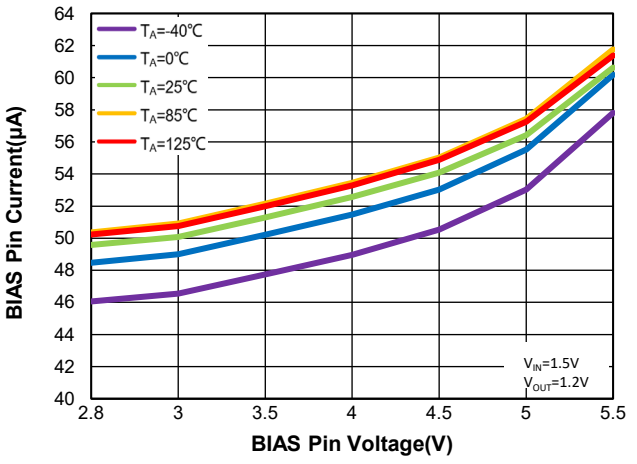


Figure 42. WR0513-12F14R
BIAS Pin Current vs. V_{BIAS} & Ambient Temperature

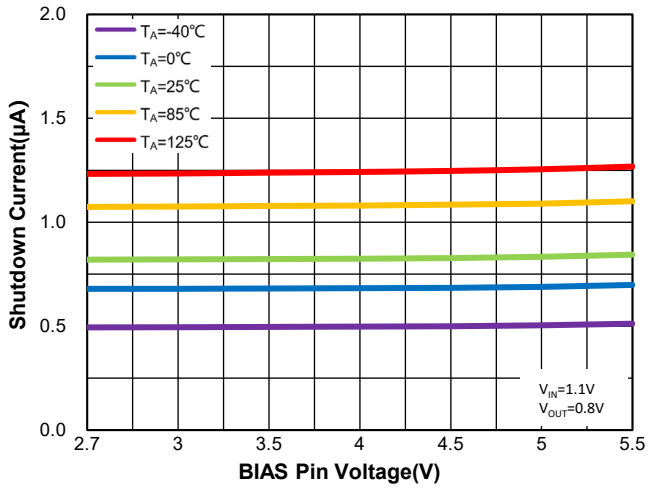


Figure 43. WR0513-ADF16R (0.8V)
Shutdown Current vs. V_{BIAS} & Ambient Temperature

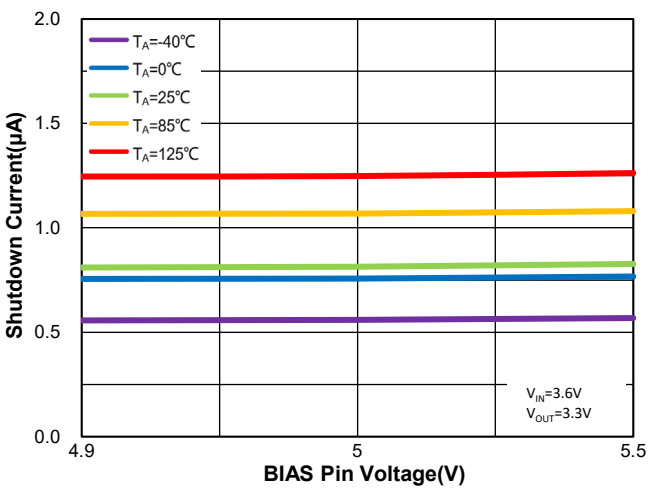


Figure 44. WR0513-ADF16R (3.3V)
Shutdown Current vs. V_{BIAS} & Ambient Temperature

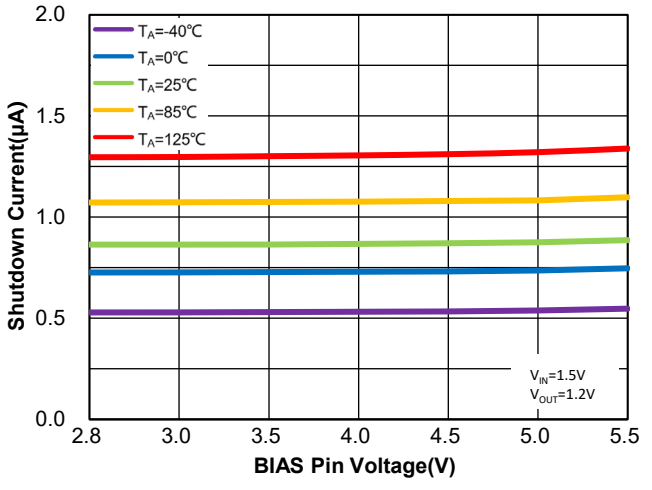


Figure 45. WR0513-12F14R
Shutdown Current vs. V_{BIAS} & Ambient Temperature

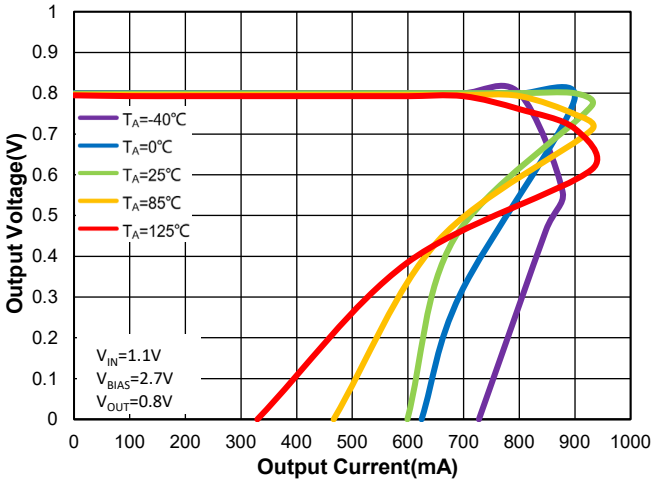


Figure 46. WR0513-ADF16R (0.8V)
Foldback Current Limit vs. I_{OUT} & Ambient Temperature

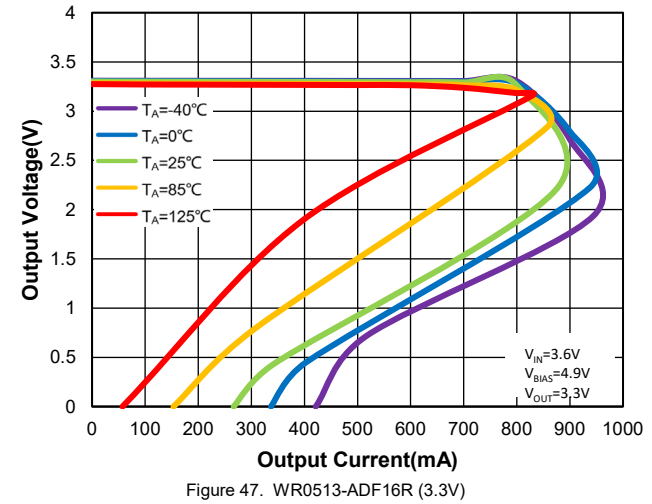


Figure 47. WR0513-ADF16R (3.3V)
Foldback Current Limit vs. I_{OUT} & Ambient Temperature

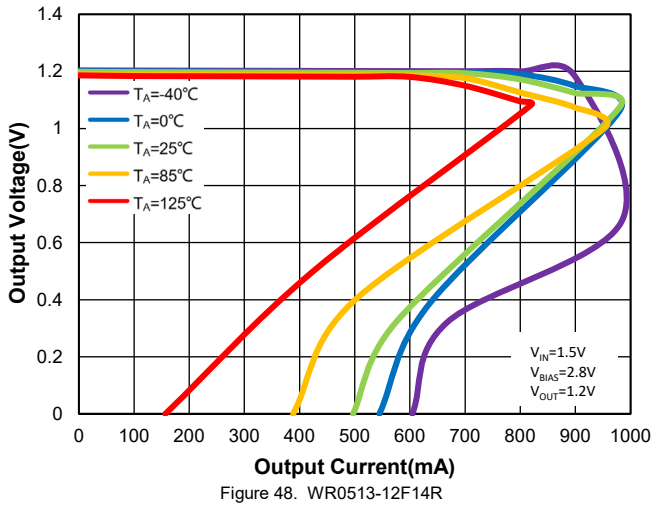


Figure 48. WR0513-12F14R
Foldback Current Limit vs. I_{OUT} & Ambient Temperature

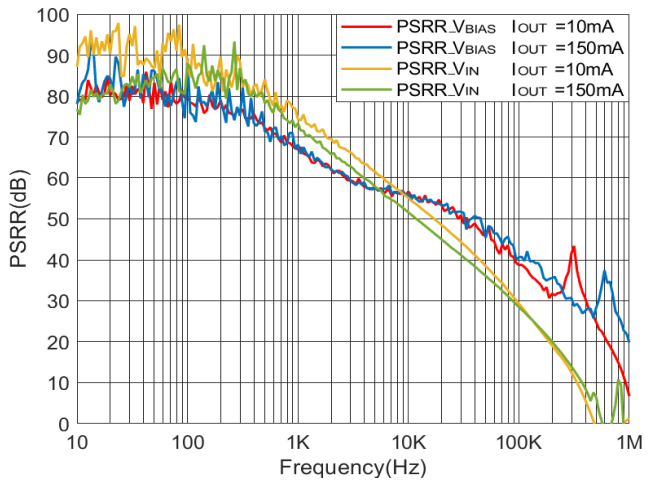


Figure 49. WR0513-ADF16R (0.8V)
Power-Supply Rejection Ratio vs. Frequency

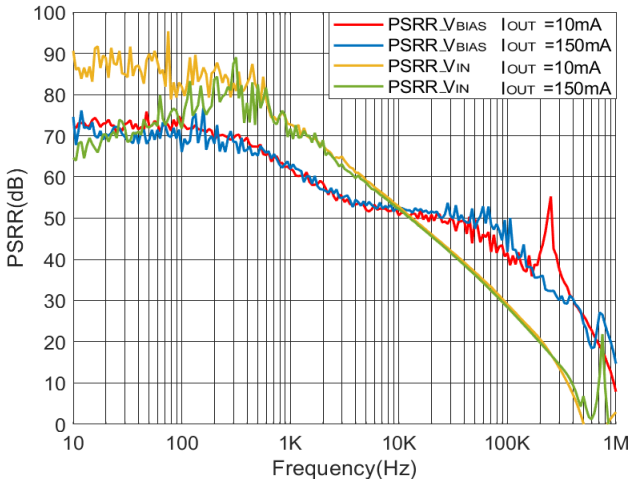


Figure 50. WR0513-ADF16R (3.3V)
Power-Supply Rejection Ratio vs. Frequency

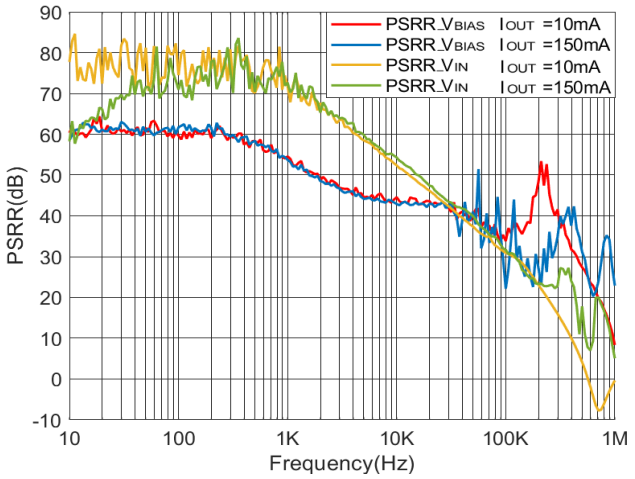


Figure 51. WR0513-12F14R
Power-Supply Rejection Ratio vs. Frequency

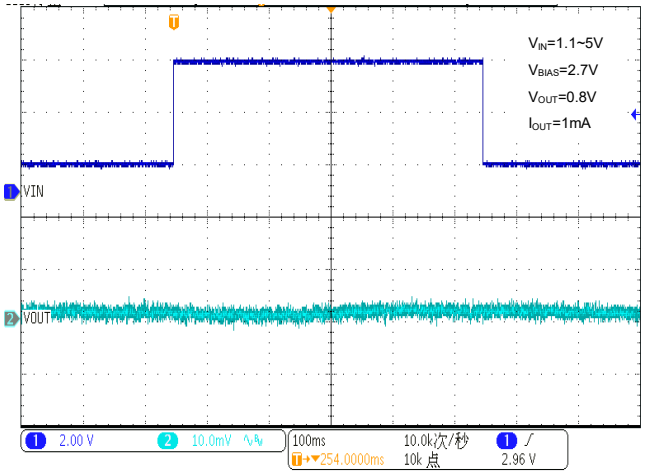


Figure 52. WR0513-ADF16R (0.8V)
Line Transient _ V_{IN}

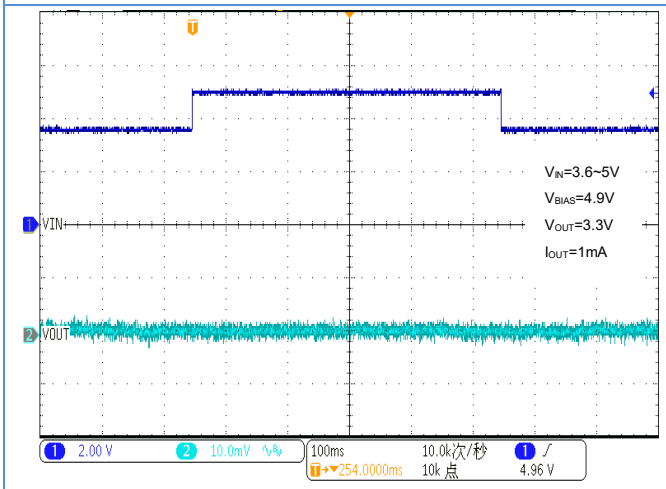


Figure 53. WR0513-ADF16R (3.3V)
Line Transient _ V_{IN}

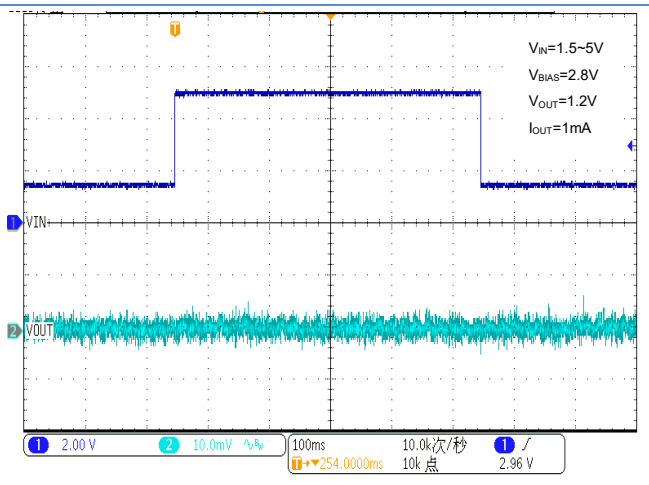


Figure 54. WR0513-12F14R
Line Transient _ V_{IN}

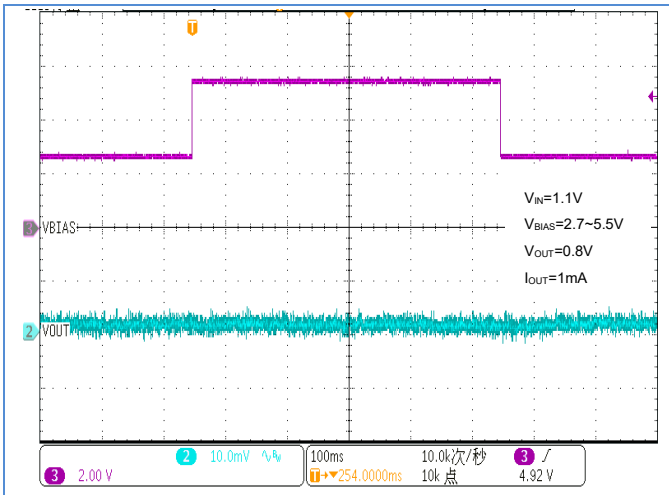


Figure 55. WR0513-ADF16R (0.8V)
Line Transient _ V_{BIAS}

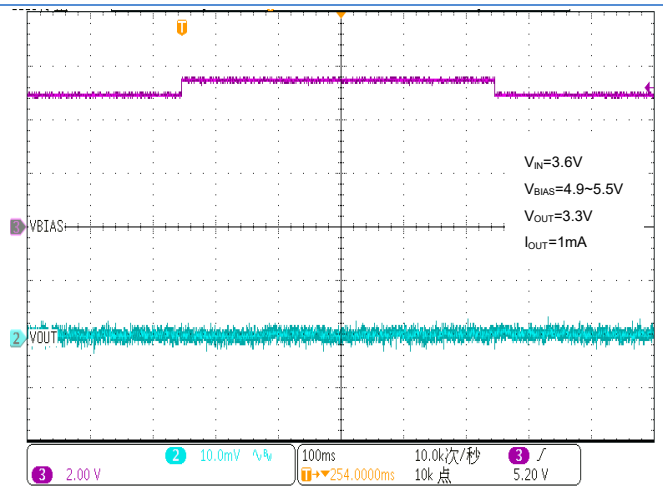


Figure 56. WR0513-ADF16R (3.3V)
Line Transient _ V_{BIAS}

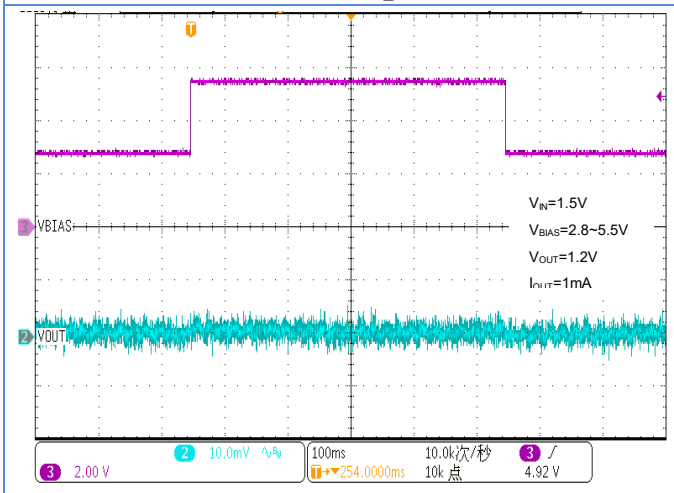


Figure 57. WR0513-12F14R
Line Transient _ V_{BIAS}

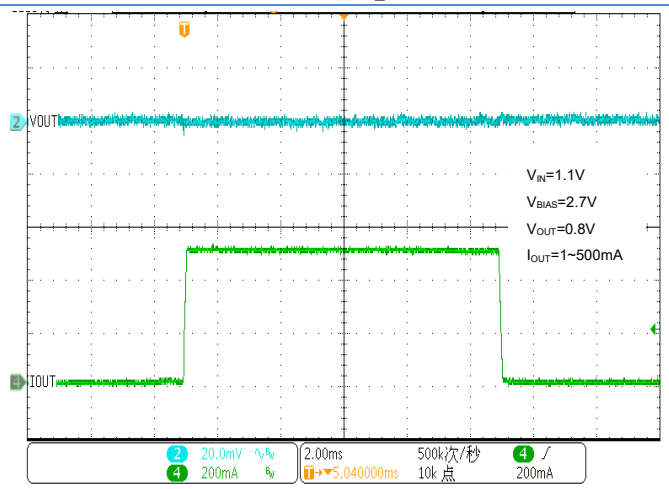


Figure 58. WR0513-ADF16R (0.8V)
Load Transient

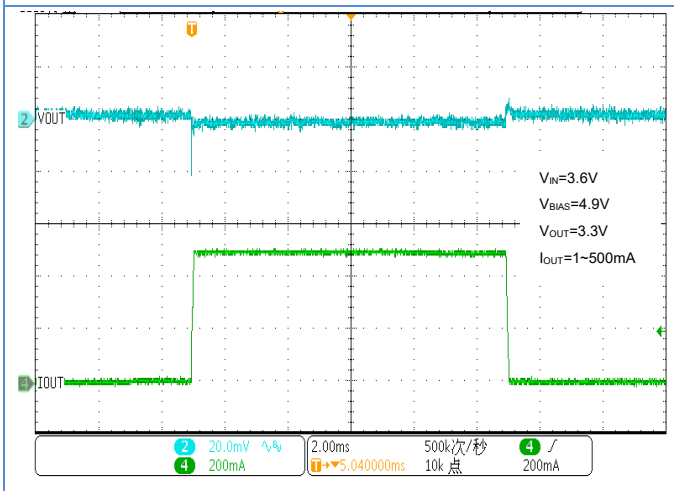


Figure 59. WR0513-ADF16R (3.3V)
Load Transient

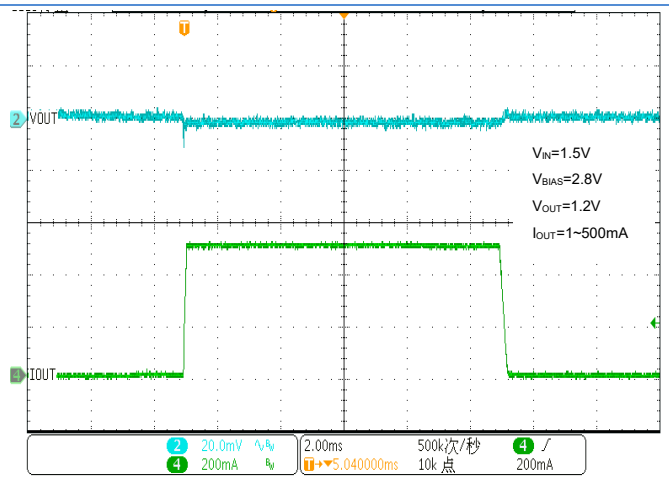


Figure 60. WR0513-12F14R
Load Transient

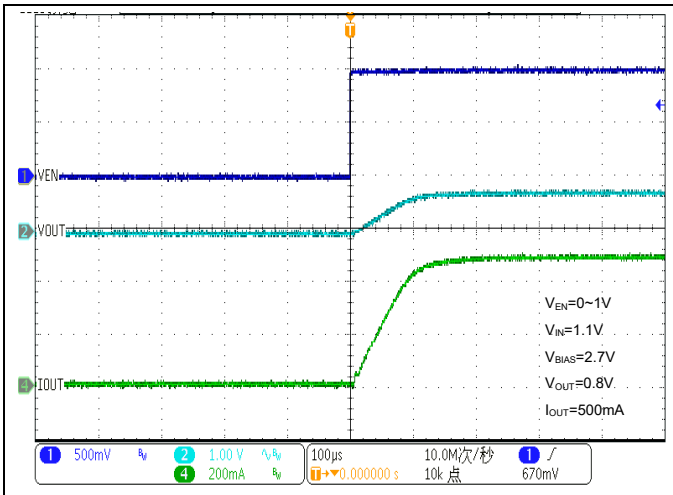


Figure 61. WR0513-ADF16R (0.8V)
Startup with EN

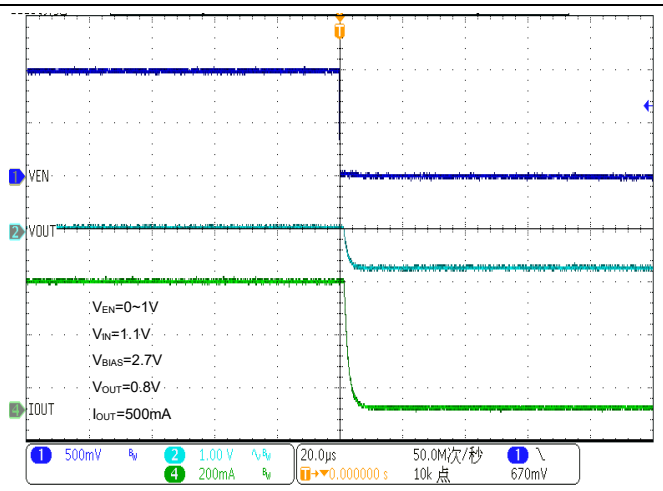


Figure 62. WR0513-ADF16R (0.8V)
Shutdown Response with Enable

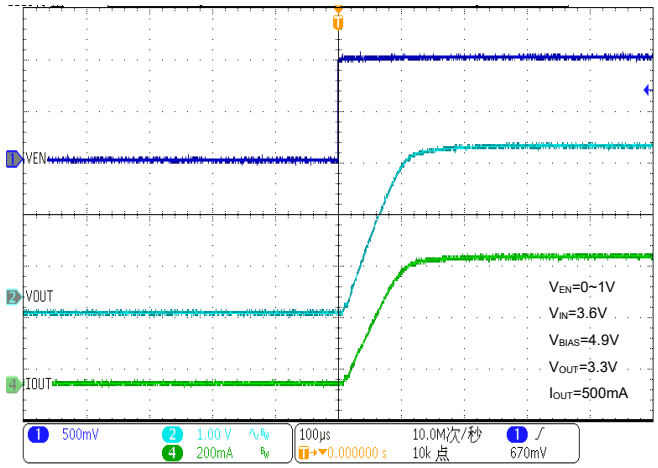


Figure 63. WR0513-ADF16R (3.3V)
Startup with EN

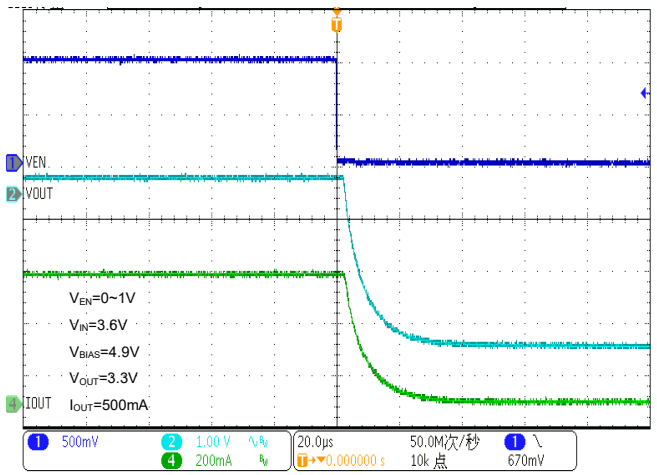


Figure 64. WR0513-ADF16R (3.3V)
Shutdown Response with Enable

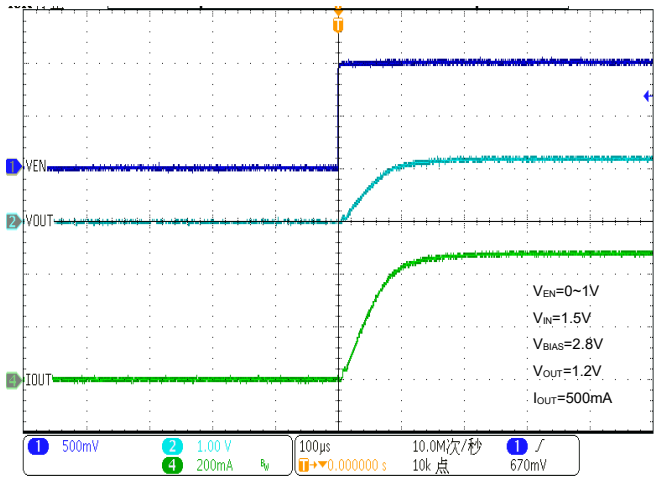


Figure 65. WR0513-12F14R
Startup with EN

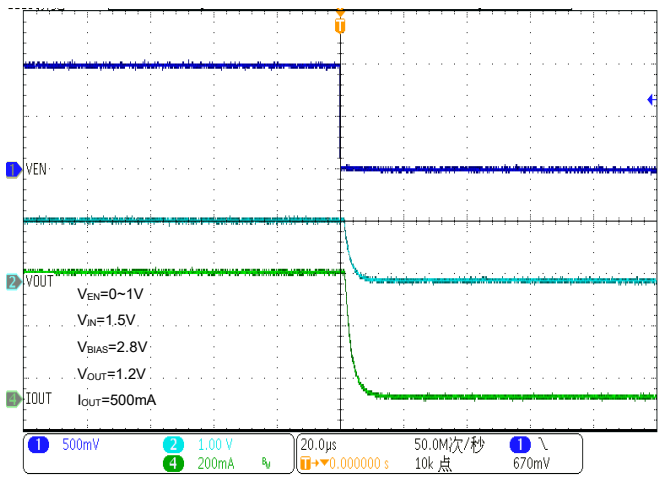


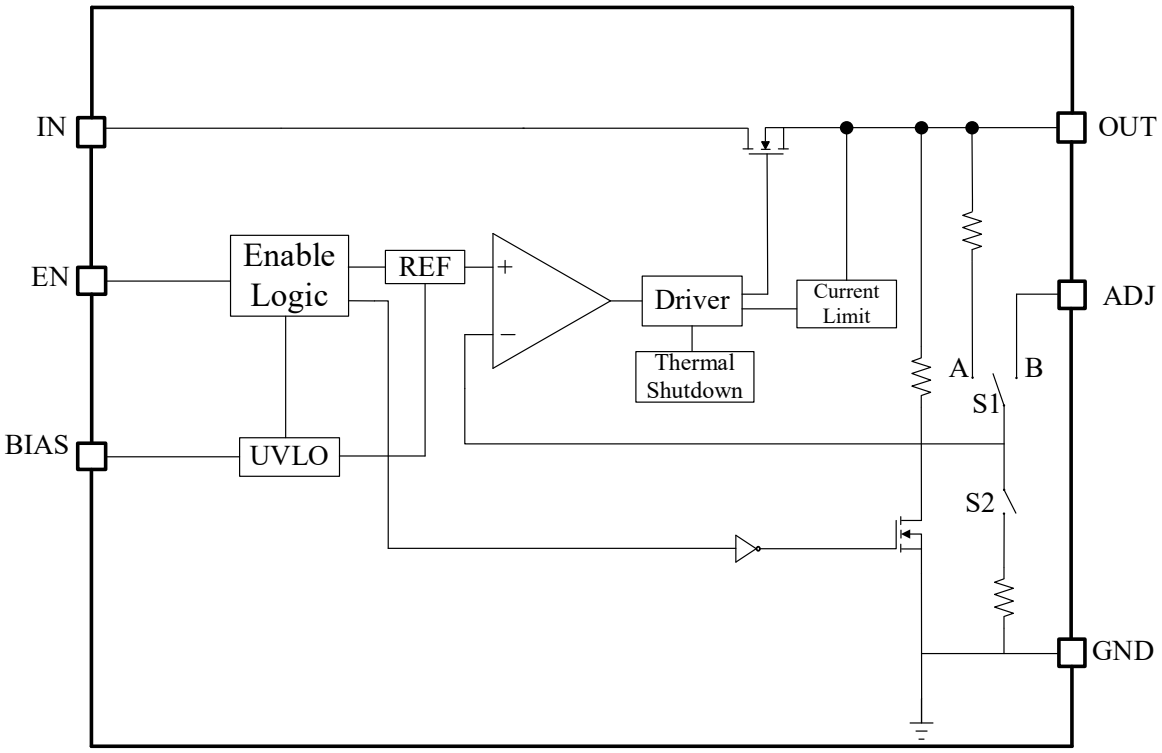
Figure 66. WR0513-12F14R
Shutdown Response with Enable

11. Function Description

11.1 Overview

The WR0513 series are high performance positive voltage regulators with separated bias voltage (V_{BIAS}), offering output current up to 500mA with low dropout voltage and very low quiescent current for portable applications. The feature of ultra-low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. In addition, the WR0513 series consist of an accurate voltage-reference block, Driver block, an error amplifier, a voltage-setting resistor net, a NMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit. The device is available in the DFN1.2X1.2-6L, DFN1.2X1.2-4L package.

11.2 Block Diagram



NOTE: Fixed version: S1 to A and S2 closed, Adjustable version: S1 to B, S2 open.

11.3 Feature Description

11.3.1 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. The WR0513 features an output voltage accuracy of 1.5% that includes the errors introduced by the internal reference, load regulation, and line regulation variance across the full range of rated load and line operating conditions over temperature, as specified by the Electrical Characteristics table. Output voltage accuracy also accounts for all variations between manufacturing lots.

11.3.2 Enable (EN)

The WR0513 EN pin has internal pull−down current source with value of 500 nA typ. When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device output shutdown. If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 BIAS Voltage (V_{BIAS})

The VBIAS power supply IQ for the LDO control circuit is very low and its input voltage must be above 2.7V or 1.6V above the normal output voltage. VBIAS provides the bias input voltage for the internal error amplifier and reference circuit, which is controlled by the internal undervoltage module. When the bias voltage is greater than the undervoltage threshold, the chip outputs normally; otherwise, the output is abnormal.

11.3.4 Dropout Voltage (V_{DO})

The WR0513 is an ultra-low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the VIN-VOUT at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the RDS (ON) of the pass-FET.

The RDS (ON) is calculated as follows:

$$R_{DS\ (ON)}=V_{DO}/I_{RATED}$$

11.3.5 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$\mathbf{PSRR = 20log\ (Ripple(in)\ /\ Ripple(out))}$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0513 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.6 Noise

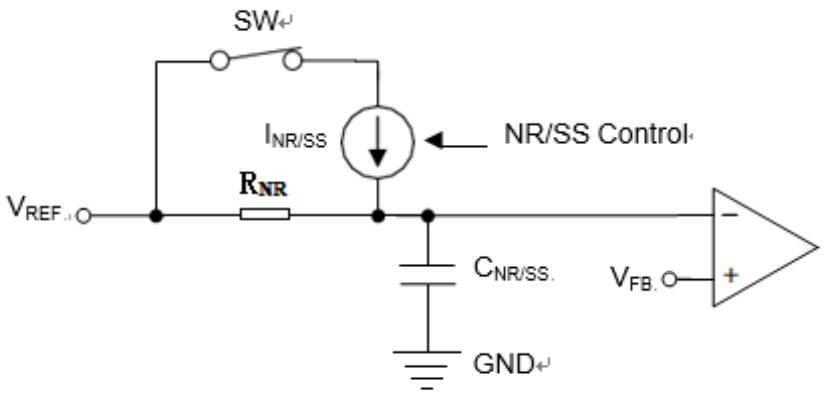
LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimizing noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR0513 has a low noise reference, high PSRR to ensure that output noise is reduced during normal operation.

11.3.7 Output Soft-Start

Soft-start is the ramping characteristic of the output voltage during the LDO turn-on period after EN and UVLO have exceeded the threshold, preventing the damage caused by output voltage overshoot to the subordinate circuits and enabling effective protection of the secondary circuits. The soft-start ramp can be programmed using a noise reduction capacitor (CNR/SS). A larger value of noise reduction capacitor will reduce noise, but will also result in a slower output turn-on ramp. Higher currents allow a reasonable start-up time to be maintained with a larger noise reduction capacitor.



Soft-Start Circuit

11.3.8 Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{SHORT}.

The WR0513 uses a constant current limiting mode where the final current is around 900mA, thus providing good protection to the device.

11.3.9 Thermal Protection

The WR0513 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (TJ) of the energized crystal exceeds 170°C (typical). The thermal shutdown hysteresis ensures that the LDO recover when the temperature drops to 145°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0513's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0513 into a thermal shutdown state will reduce the reliability of the device.

For reliable operation, limit the junction temperature to a maximum of 125°C. The thermal margin in a given layout is to be estimated. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition of the application.

11.4 Functional Mode Of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V \geqslant V_{IN} > V_{OUT(nom)} + V_{DO}$	$5.5V \geqslant V_{BIAS} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{UVLO} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{UVLO} < V_{BIAS} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{BIAS} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(nom)}$ + V_{DO}) and is less than 5.5V.
2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.
3. The output current is less than the current limit (I_{OUT} < I_{CL}).
4. The device junction temperature is less than the thermal shutdown temperature (T_J < T_{sd}).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

11.4.3 Disabled

The WR0513 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.4V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0513 is a linear voltage regulator with an input voltage of 1.1 V to 5.5 V and an output voltage of 0.6 V to 3.6 V. The accuracy is 1.5% for V_{REF} voltages. The maximum output current is 500 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Start-Up

12.1.1.1 Enable (EN)

The WR0513 can determine the output of the device through the EN input voltage, EN is higher than the voltage threshold to turn on, in order to prevent the device from turning off when the input voltage drops during the turn-on period, EN has a certain hysteresis. WR0513 internal EN to GND has a pull-down current source, the pull-down current is about 500nA, when EN floats default to low, if you do not need EN independent control, it is recommended to connect EN directly to IN. If you want to use the EN control, you need to give a control voltage to the EN side.

12.1.1.2 Automatic Discharge

The WR0513 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.1.3 Soft-Start

Soft start refers to the characteristic that the output voltage rises gradually as the EN voltage jumps from low to high. Reducing the output voltage rise rate reduces the inrush current that charges the output capacitor. The inrush current is the current entering the LDO during startup and consists of the load current, the current charging the output capacitor, and the ground pin current.

The inrush current can be estimated by the following equation:

$$I_{OUT}(t) = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right)$$

The WR0513 controls soft-start through an external capacitor (CNR/SS), which helps to reduce inrush current and reduce load transients on the input power bus, thus solving startup initialization problems that can result when powering FPGAs, DSPs, or other high-current loads.

12.1.2 Capacitor Recommendation

The WR0513 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN}, V_{BIAS} and V_{OUT} pins to improve their stability. The use of multilayer ceramic capacitors is recommended. These capacitors also have limitations. Ceramic capacitors with X7R-, X5R- and COG grade dielectric materials have relatively good capacitive stability at different temperatures. The WR0513 is designed to use 1μF ceramic capacitors at the input, 0.1μF ceramic capacitors at BIAS and 2.2μF or larger ceramic capacitors at the output. Place C_{IN}, C_{BIAS} and C_{OUT} as close as possible to the IN, BIAS and OUT pins to minimize the tracking inductance from the capacitors to the device.

Increasing the capacitance at the input and bias side will reduce the transient input drop and load current at startup. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors may cause unwanted ringing at the output, which requires careful design of short interconnections to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of a few hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to step changes in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but also reduces the control loop bandwidth, which slows down the response time.

Because, the LDO cannot consume charge, when the output load is removed or greatly reduced, the control loop must close via the FET and wait for any excess charge to be depleted.

12.1.3 Power Dissipation (P_D)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

PD can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage. The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Detailed Design Procedure

The adjustable version of WR0513 has a thermally stable reference voltage of 0.8 ± 0.004V， the voltage on the ADJ pin sets the output voltage which is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Using lower values for R1 and R2 is recommended to reduce the noise injected from the FB pin. Note that R1 is connected from V_{OUT} pin to ADJ pin, and R2 is connected from ADJ to GND.

$$R_1 = R_2 * \left(\frac{V_{OUT}}{0.8V} - 1\right)$$

In order to get better load regulation, R1 must be connected very close to the OUT and ADJ pin, while the ground of R2 must be as close as possible to the ground pin of the chip.

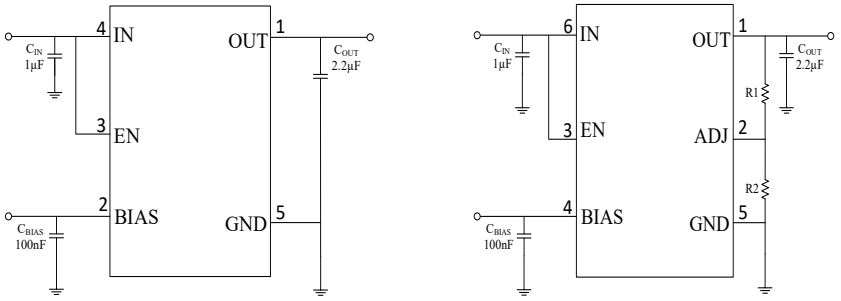
Suggested Component Values

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
1.2	20	40
1.8	20	16
2.5	20	9.4
3.3	20	6.4

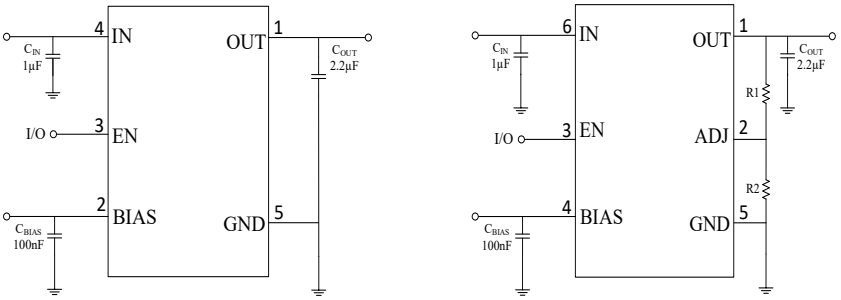
12.2 Typical Application

This section discusses the application of the WR0513 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic 1: V_{OUT} normally open, no control.



Circuit schematic 2: V_{OUT} control by external voltage to EN.



C_{IN}, C_{BIAS} and C_{OUT} should be selected with the recommended appropriate capacitance. 1μF ceramic capacitors for C_{IN}, 2.2μF for C_{OUT} and 100nF for C_{BIAS} should be selected to help balance the charge required to charge the output capacitor at start-up, thus reducing the input voltage drop.

13. Power supply recommendation

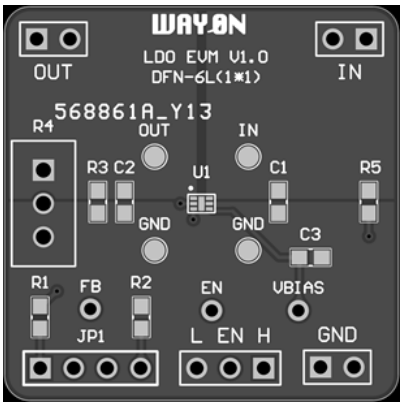
The WR0513 has a V_{IN} range of between 1.1 V and 5.5 V and an input capacitance of 1μF. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

Layout Example：



15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
WR0513	DFN-4L	WAYON LDO EVM V1.0 - DFN1.2×1.2-4L
	DFN-6L	WAYON LDO EVM V1.0 -DFN1.2×1.2-6L

16. Naming conventions

WR AA BB-CC DDD E

W R: WAYON Regulator

A A: 05 - Output Current 500 mA

B B: Serial number

C C: Output Voltage/AD-Output Voltage, Adjustable Voltage

DDD: FF4- Package, DFN-4

FF6- Package, DFN-6

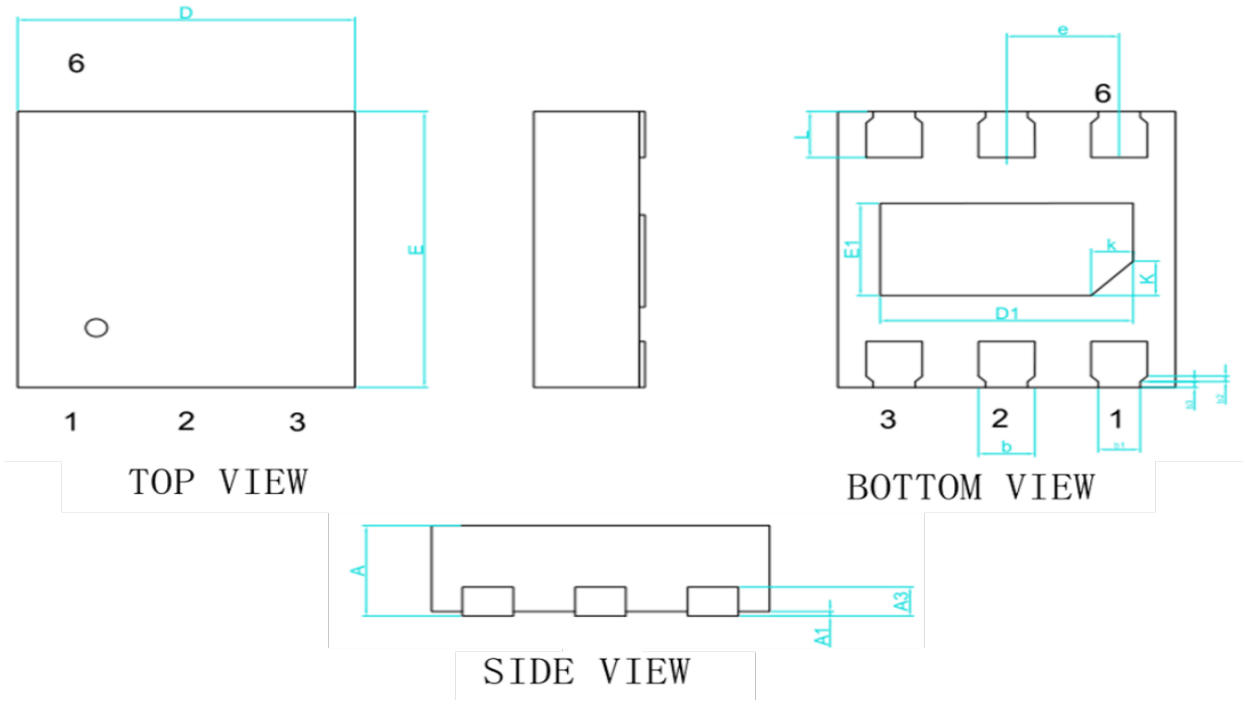
E: R-Reel & T-tube

17. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

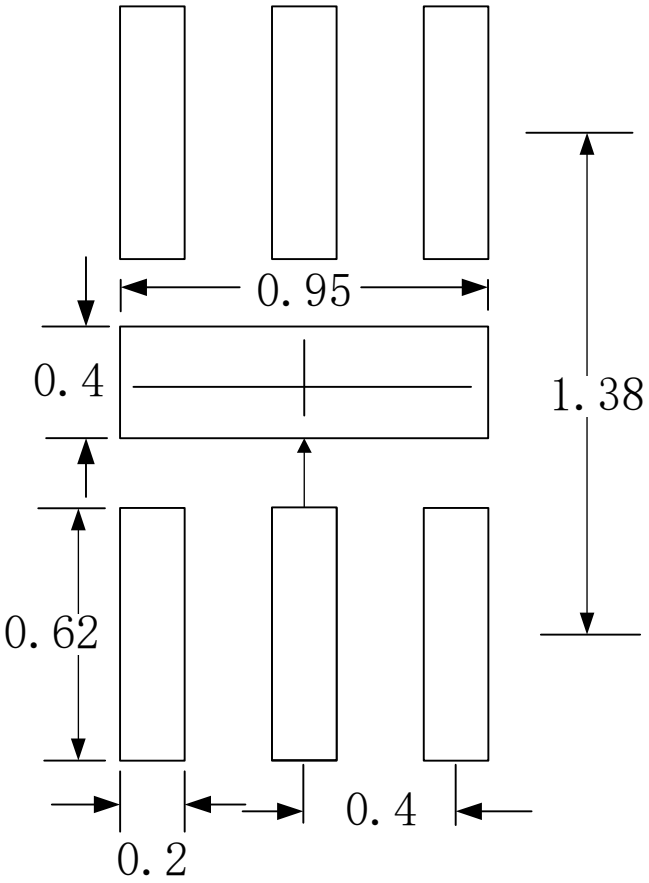
18. Package Information

DFN1.2*1.2-6L



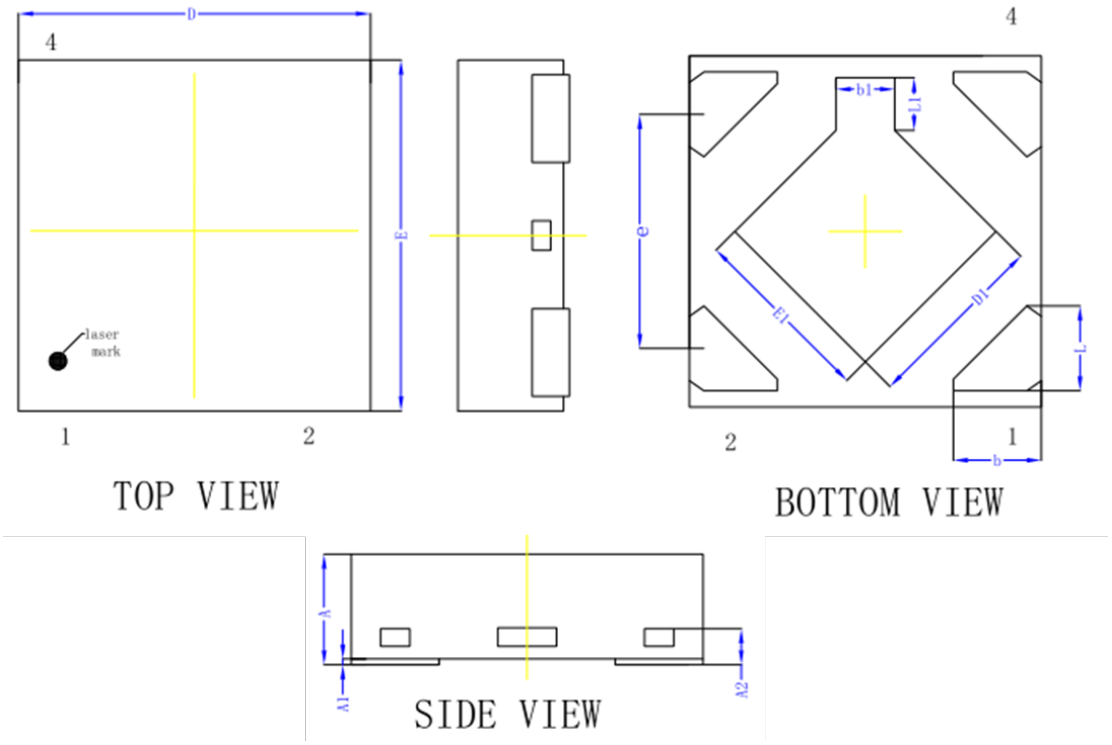
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	-	0.02
A3		0.127REF	
D	1.15	1.20	1.25
E	1.15	1.20	1.25
D1	0.85	0.95	1.05
E1	0.35	0.40	0.45
k		0.15REF	
e		0.40REF	
b		0.20REF	
b1		0.15REF	
b2		0.025REF	
b3		0.025REF	
L	0.15	0.20	0.25

Suggested Pad Layout: DFN1.2*1.2-6L



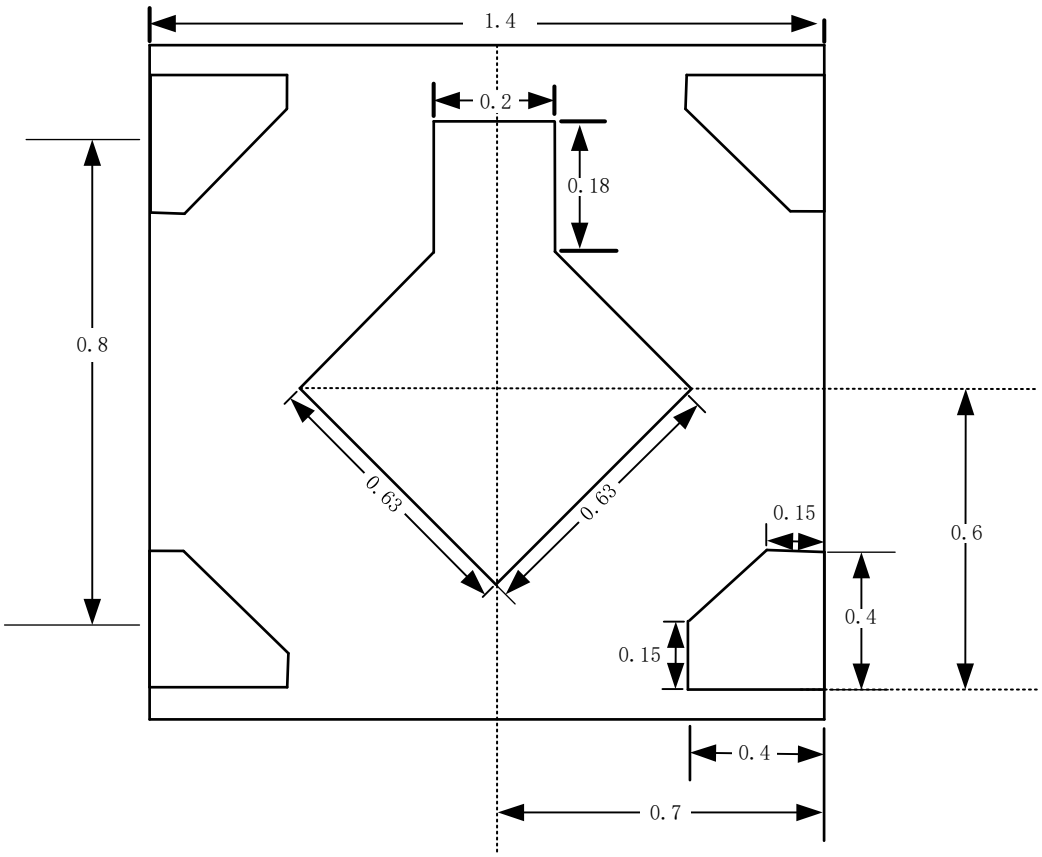
NOTE: Dimensions In Millimeters

DFN1.2*1.2-L



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
e		0.800BSC	
A2		0.127REF	
D	1.15	1.20	1.25
E	1.15	1.20	1.25
D1	0.58	0.63	0.68
E1	0.58	0.63	0.68
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
L	0.25	0.30	0.35
L1	0.13	0.18	0.23

Suggested Pad Layout: DFN1.2*1.2-L



NOTE: Dimensions In Millimeters

19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking
WR0513-06F16R	0.6V	DFN1212-6	3k/Reel	513 06
WR0513-08F16R	0.8V	DFN1212-6	3k/Reel	513 08
WR0513-09F16R	0.9V	DFN1212-6	3k/Reel	513 09
WR0513-10F16R	1.0V	DFN1212-6	3k/Reel	513 10
WR0513-105F16R	1.05V	DFN1212-6	3k/Reel	513 105
WR0513-11F16R	1.1V	DFN1212-6	3k/Reel	513 11
WR0513-12F16R	1.2V	DFN1212-6	3k/Reel	513 12
WR0513-15F16R	1.5V	DFN1212-6	3k/Reel	513 15
WR0513-18F16R	1.8V	DFN1212-6	3k/Reel	513 18
WR0513-25F16R	2.5V	DFN1212-6	3k/Reel	513 25
WR0513-28F16R	2.8V	DFN1212-6	3k/Reel	513 28
WR0513-30F16R	3.0V	DFN1212-6	3k/Reel	513 30
WR0513-33F16R	3.3V	DFN1212-6	3k/Reel	513 33
WR0513-ADF16R	Adjustable	DFN1212-6	3k/Reel	513 AD
WR0513-06F14R	0.6V	DFN1212-4	3k/Reel	513 06
WR0513-08F14R	0.8V	DFN1212-4	3k/Reel	513 08
WR0513-09F14R	0.9V	DFN1212-4	3k/Reel	513 09
WR0513-10F14R	1.0V	DFN1212-4	3k/Reel	513 10
WR0513-105F14R	1.05V	DFN1212-4	3k/Reel	513 105
WR0513-11F14R	1.1V	DFN1212-4	3k/Reel	513 11
WR0513-12F14R	1.2V	DFN1212-4	3k/Reel	513 12
WR0513-15F14R	1.5V	DFN1212-4	3k/Reel	513 15
WR0513-18F14R	1.8V	DFN1212-4	3k/Reel	513 18
WR0513-25F14R	2.5V	DFN1212-4	3k/Reel	513 25
WR0513-28F14R	2.8V	DFN1212-4	3k/Reel	513 28
WR0513-30F14R	3.0V	DFN1212-4	3k/Reel	513 30
WR0513-33F14R	3.3V	DFN1212-4	3k/Reel	513 33

STATEMENTS

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

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WAYON website: http://www.way-on.com

For additional information, please contact your local Sales Representative.

Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.

Users should verify actual device performance in their specific applications.