WR0512
Ultra-low Dropout, 500mA, CMOS LDO

1. General Descriptions

The WR0512 series are ultra-low dropout, Low quiescent current, high PSRR CMOS LDO. The dropout voltage is 130mV (Typ.) at 500mA load current.

Using CMOS construction, the quiescent current consumed by the WR0512 is typically 60μA over the entire input voltage range, making it attractive for consumer, networking applications that demand high output current. The WR0512 series are available in wide output voltage range version from 1.2V to 3.3V with 0.1V step.

The WR0512 series offer thermal shutdown (OTP) and current limit functions, to assure the stability of chip and power system at wrong condition, and it uses trimming technique to guarantee output voltage accuracy within ±2%.

The WR0512 regulators are available in SOT-23-3、 SOT-23-5 、 SOT-89-3/L packages. Standard products are Pb-free and Halogen-free.

2. Features

- PSRR : 70dB@1KHz
- Output Current: 500mA
- Input Voltage: 2.5V to 5.5V
- Output Voltage: 1.2V to 3.3V
- Dropout Voltage: 130mV @ I_{OUT} = 500mA
- Quiescent Current: 60μA (Typical)
- Shut-down Current: < 1μA
- Recommend Capacitor: 4.7μF
- Operating Temperature: -40 to +85ºC
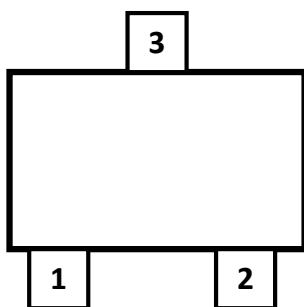- Output Noise: 120μVRMS

3. Applications

- LCD TV
- STB
- Computer, Graphic card
- Network communication equipments
- Others portable electronic device
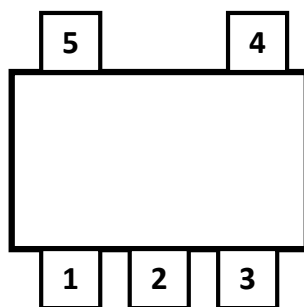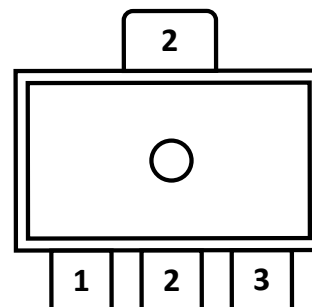
4. Typical Application
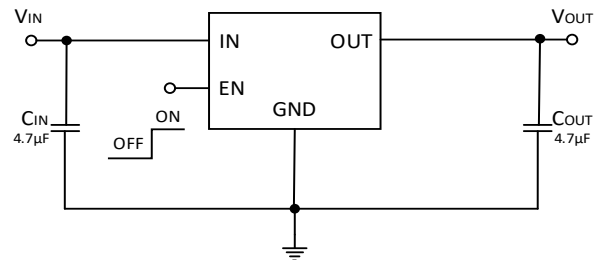
5. Pin Configuration

(Top View)

SOT23-3   SOT23-5   SOT89-3/L

6. Pin Description

PIN NUMBER				PIN NAME	I/O	PIN FUNCTIONS
SOT23-3	SOT23-5	SOT89-3	SOT89-3L			
3	1	2	3	IN	I	Input voltage supply. Bypass with a typical 4.7µF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.
1	2	1	2	GND	-	Common ground.
-	3	-	-	EN	I	Enable input. Active High. EN includes a small pull-up current source, nominally 0.1µ A.
-	4	-	-	NC	-	NC.
2	5	3	1	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 4.7µF is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible.

7. Absolute Maximum Ratings[1]

PARAMETER		RATING	UNIT
Input voltage range		-0.3 to 6.5	V
EN Input voltage range		-0.3 to V_{IN}	V
Output voltage range		-0.3 to V_{IN}	V
Power Dissipation PD @T_A = 25ºC	SOT23-3 & SOT23-5	500	mW
	SOT89-3/L	625	mW
Thermal resistance[2] [4] $R_{\theta JA}$	SOT23-3 & SOT23-5	250	℃/W
	SOT89-3/L	200	℃/W
Top Thermal resistance[2] [3] $R_{\theta JC}$	SOT23-5	120	℃/W
Junction Temperature		150	℃
Lead Temperature Range		260	℃
Storage Temperature Range		-55 to 150	℃
ESD Susceptibility	HBM	±4000	V

NOTE1: Greater than these given values, the device will be damaged.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 1 oz copper, no via holes on GND copper.

NOTE3: Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

NOTE4: Power dissipation is calculate by $P_{D(MAX)} =(T_J -T_A) / R_{\theta JA}$.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	2.5 to 5.5	V
EN Input voltage range	1.2 to 5.5	V
Nominal output voltage range	1.2 to 3.3	V
Output current	0 to 500	mA
Input capacitor	4.7	µF
Output capacitor	4.7	µF
Operating temperature range	-40 to 85	℃

9. Electrical Characteristics $_{(V_{IN}=V_{OUT(NOMINAL)}+1V, C_{IN}=C_{OUT}=4.7\mu F, Full= -40℃ \text{ to } 85℃, \text{ unless otherwise noted})}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage Range	$V_{OUT} ≤1.5V, V_{IN}=2.5V, I_{OUT}=1mA$, Full	$0.97 V_{OUT}$	V_{OUT}	$1.03 V_{OUT}$	V
		$V_{OUT}＞1.5V, I_{OUT}=1mA$, Full	$0.98 V_{OUT}$	V_{OUT}	$1.02 V_{OUT}$	
V_{DO}	Dropout Voltage[1]	$V_{OUT}=V_{OUT}*0.98, I_{OUT}=500mA$, Full		130		mV
I_{LIMT}	Output current limit	$V_{IN}=5V$, Full		800		mA
I_{OUT}	Maximum output current in the accuracy range[2]	$V_{EN}=V_{IN}$, Full	500			mA
LNR	Line Regulation	$V_{OUT}=3.3V, V_{IN}=4.3\sim5.5V, I_{OUT}=1mA$, Full		0.1		%/V
LDR	Load Regulation[3]	$V_{OUT}=3.3V, I_{OUT}=1\sim500mA$, Full		15		mV
I_Q	Quiescent Current	$V_{OUT}=3.3V, I_{OUT}=0mA, T_A=25℃$		60	90	μA
I_{SHDN}	Shut-down Current	$V_{EN} = 0V$, Full		0.1	1.0	μA
PSRR	Power Supply Ripple Rejection	$V_{IN}=(V_{OUT}+1V)_{DC}+0.2V_{P-P}$ f=1kHz, $I_{OUT}=10mA$, @$V_{OUT}=3.3V, T_A=25℃$		70		dB
V_{NO}	Output noise voltage	BW=10Hz to 100kHz, $C_{OUT}=4.7\mu F$, $I_{OUT}=10mA, T_A=25℃$		120		μV_{RMS}
V_{ENH}	EN high voltage (enabled)	$V_{IN}=5.5V, I_{OUT}=1mA$, Full	1.2			V
V_{ENL}	EN low voltage (disabled)	$V_{IN}=5.5V, I_{OUT}=1mA$, Full			0.4	V
T_{SD}	Thermal shutdown threshold			165		ºC
ΔT_{SD}	Thermal shutdown hysteresis			30		ºC

Note1: The dropout voltage is defined as $(V_{IN}-V_{OUT})$ when V_{OUT} is $V_{OUT(NOM)}*98\%$.

Note2: Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when $V_{IN}< V_{OUT} + V_{DROP}$.

Note3: The Load regulation is measured using pulse techniques with duty cycle < 5%.

10. Typical Performance Characteristics $(T_A = -40$ to 85^oC, $V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=4.7\mu F$, unless otherwise noted)
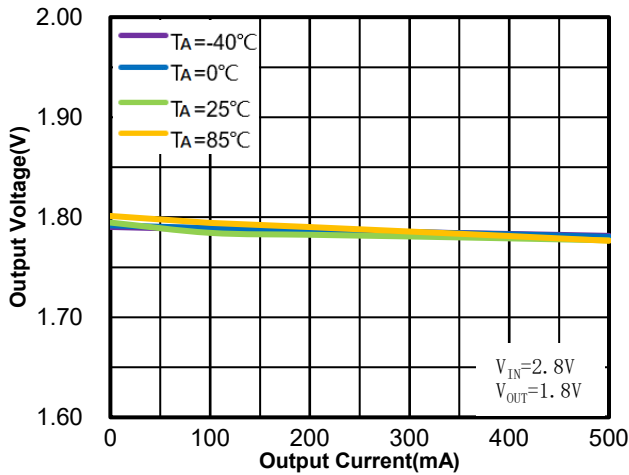

Figure 1. WR0512-18A20R
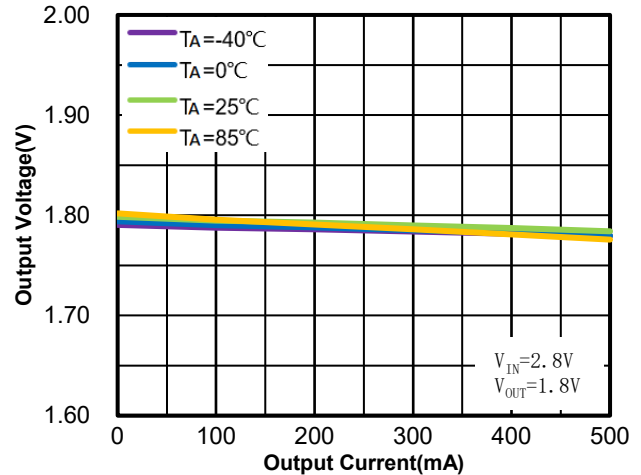Load Regulation vs. I_{OUT} & Ambient Temperature

Figure 2. WR0512-18A50R
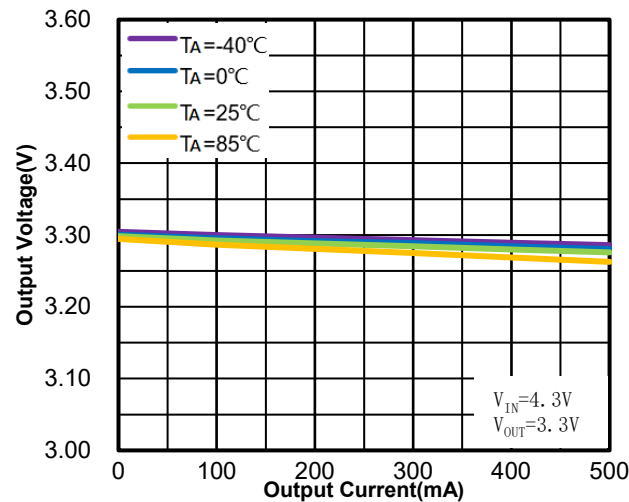Load Regulation vs. I_{OUT} & Ambient Temperature

Figure 3. WR0512-33A20R
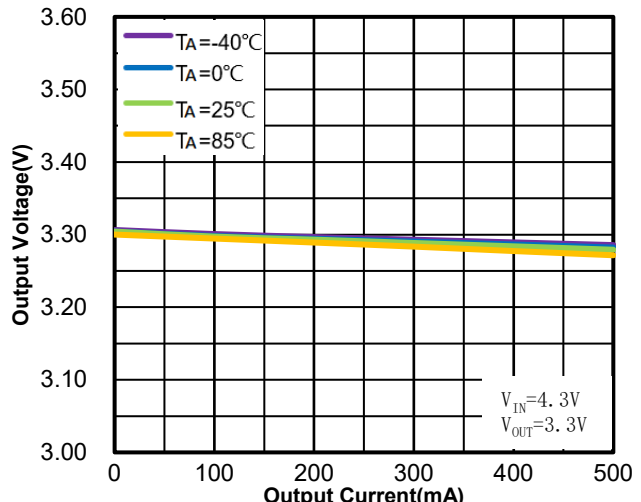Load Regulation vs. I_{OUT} & Ambient Temperature

Figure4. WR0512-33A50R
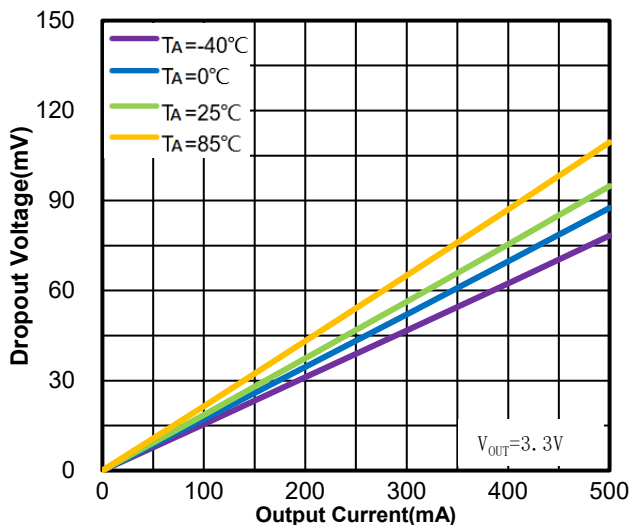Load Regulation vs. I_{OUT} & Ambient Temperature

Figure 5. WR0512-33A20R
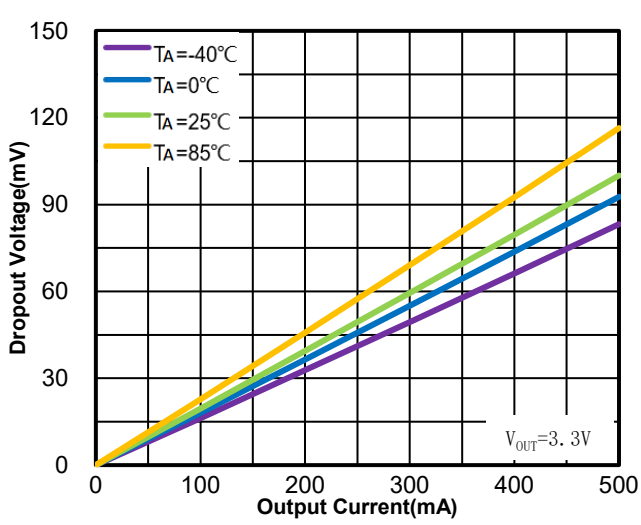Dropout Voltage vs. I_{OUT} & Ambient Temperature

Figure 6. WR0512-33A50R
Dropout Voltage vs. I_{OUT} & Ambient Temperature

Typical Performance Characteristics (T$_A$= -40 to 85ºC, V$_{IN}$=V$_{OUT}$+1V, C$_{IN}$=C$_{OUT}$=4.7μF, unless otherwise noted)
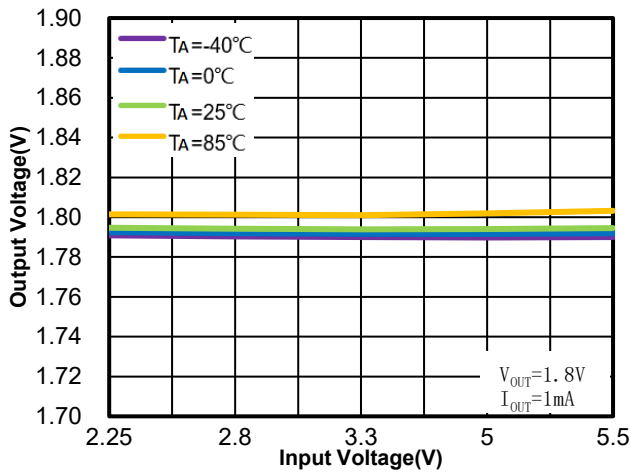

Figure 7. WR0512-18A20R
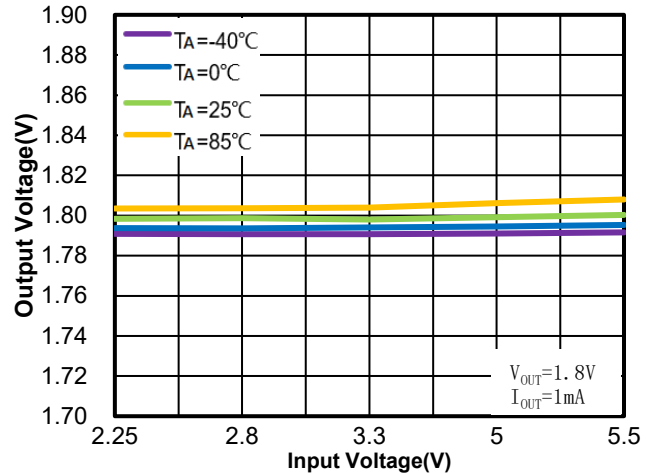Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure 8. WR0512-33A50R
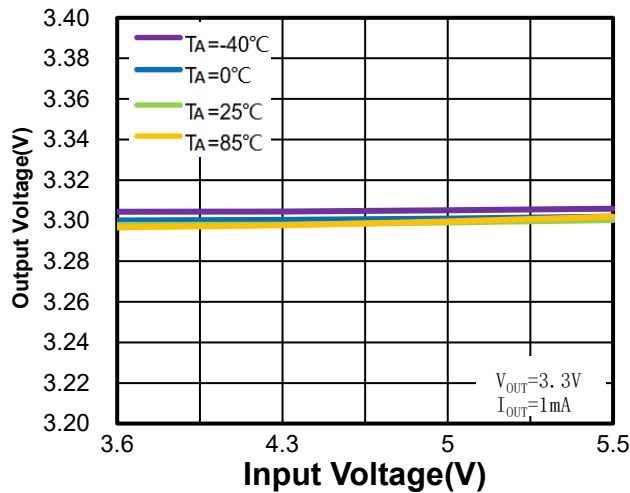Dropout Voltage vs. I$_{OUT}$ & Ambient Temperature

Figure9.WR0512-33A20R
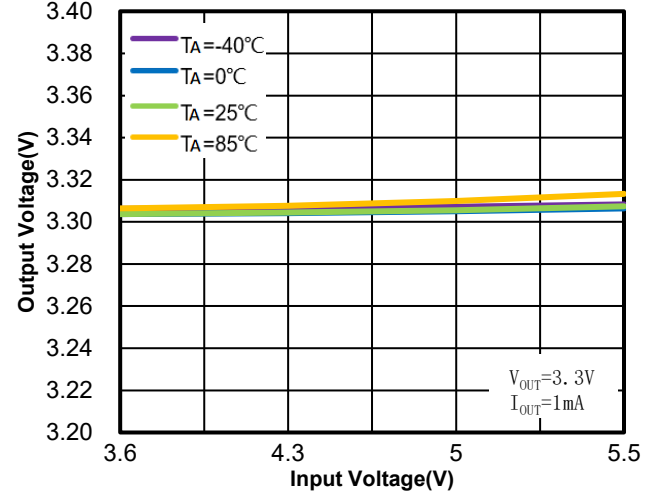Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure10.WR0512-33A50R
Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure11.WR0512-18A20R
Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure12.WR0512-18A50R
Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Typical Performance Characteristics (T$_A$= -40 to 85ºC, V$_{IN}$=V$_{OUT}$+1V, C$_{IN}$=C$_{OUT}$=4.7μF, unless otherwise noted)

Figure13.WR0512-33A20R
Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure14.WR0512-33A50R
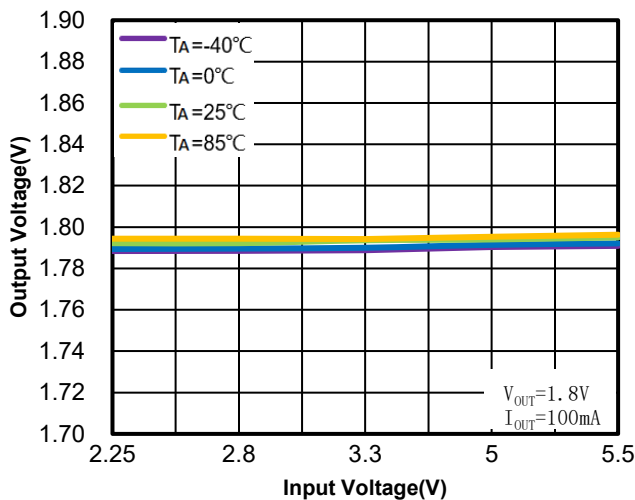Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure15.WR0512-18A20R
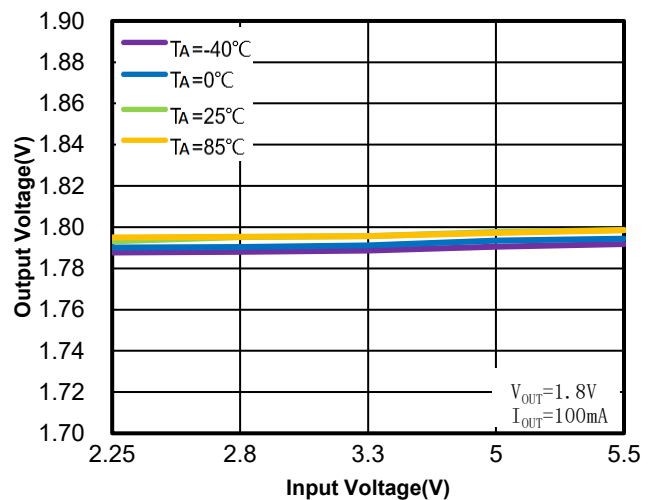Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Figure16.WR0512-18A50R
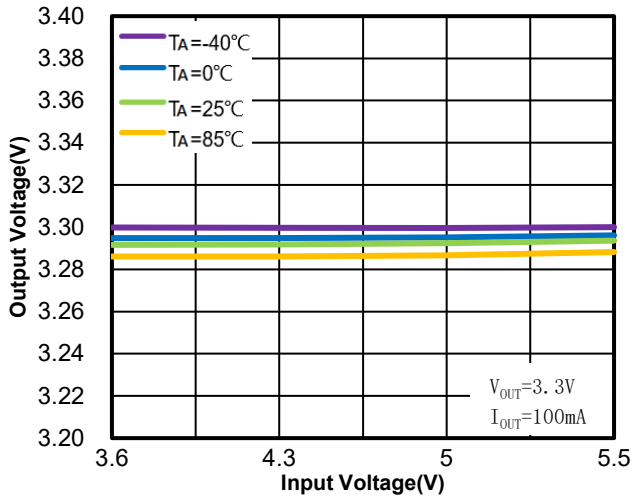Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature
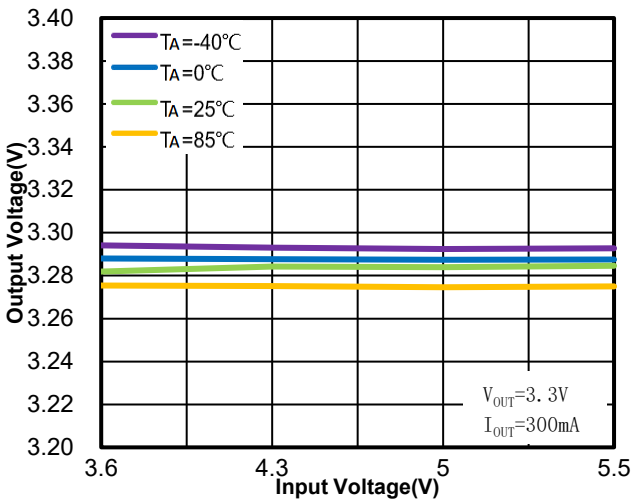
Figure17.WR0512-33A20R
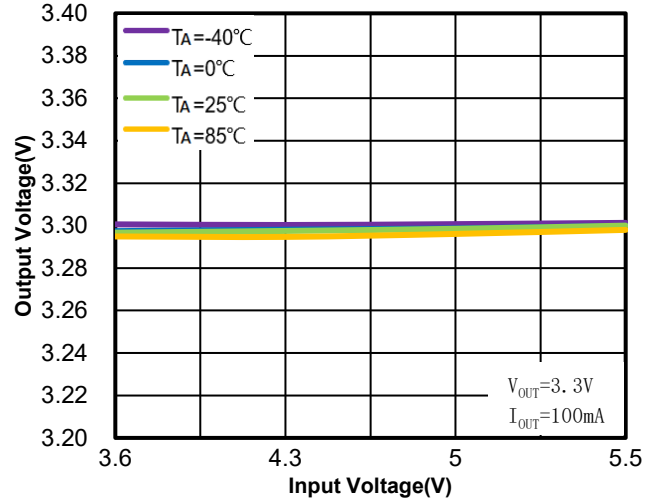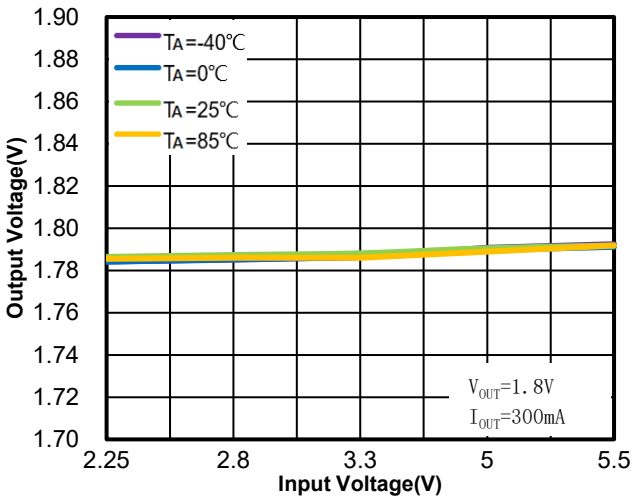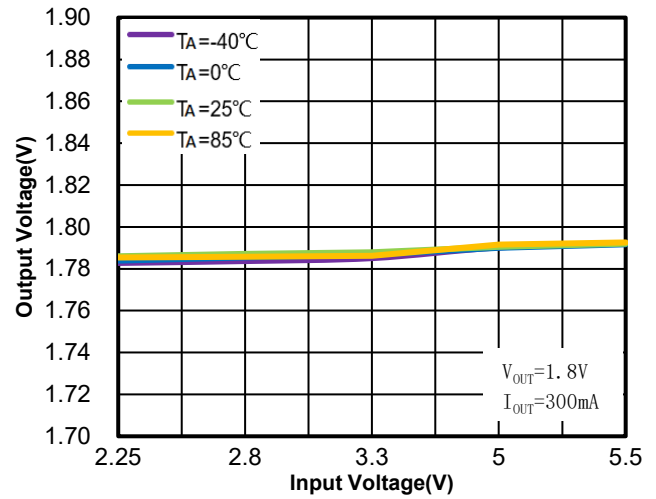Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature
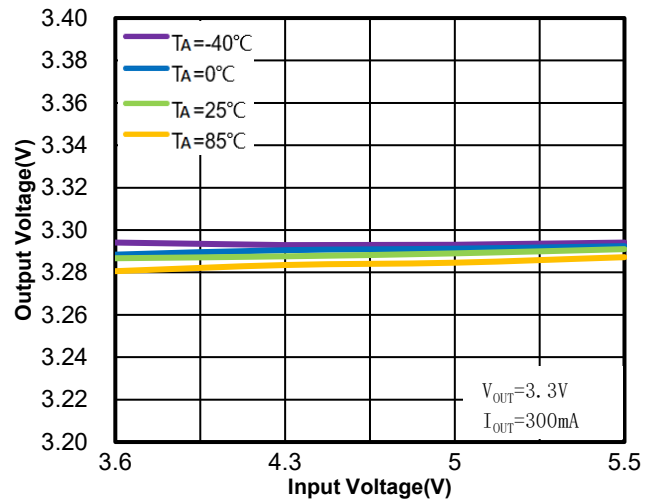
Figure18.WR0512-33A50R
Regulation vs. V$_{IN}$ (Line Regulation) & Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85°C, V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=4.7μF, unless otherwise noted)
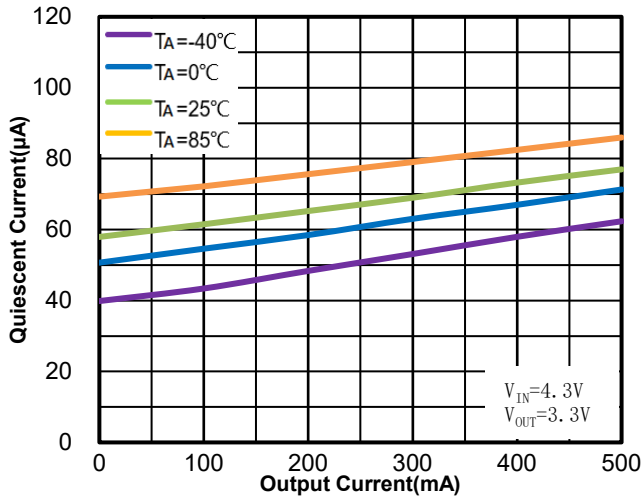
Figure19. WR0512-33A20R
Quiescent Current vs. I_{OUT} & Ambient Temperature
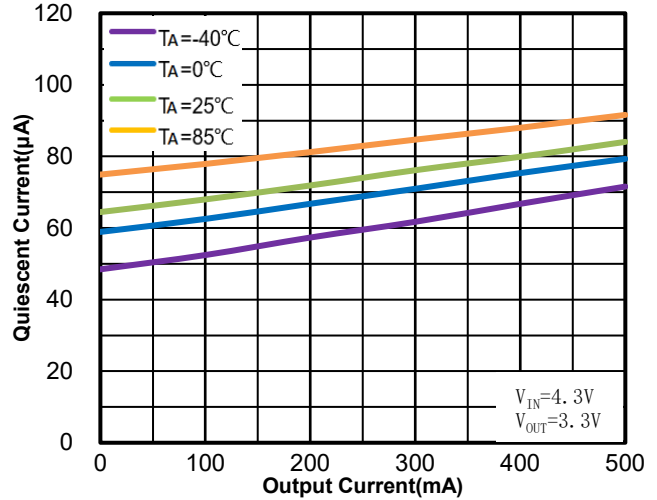
Figure 20. WR0512-33A50R
Quiescent Current vs. I_{OUT} & Ambient Temperature
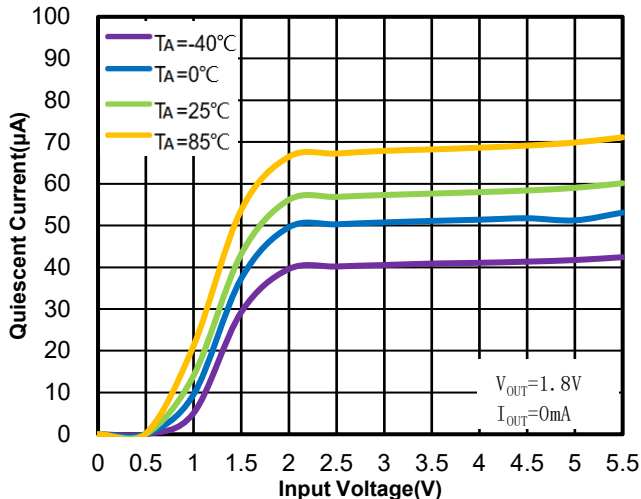
Figure 21. WR0512-18A20R
Quiescent Current vs. V_{IN} & Ambient Temperature
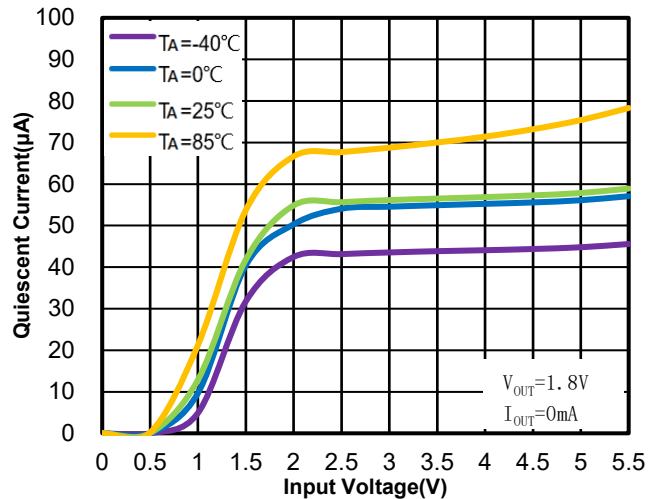
Figure 22. WR0512-18A50R
Quiescent Current vs. V_{IN} & Ambient Temperature
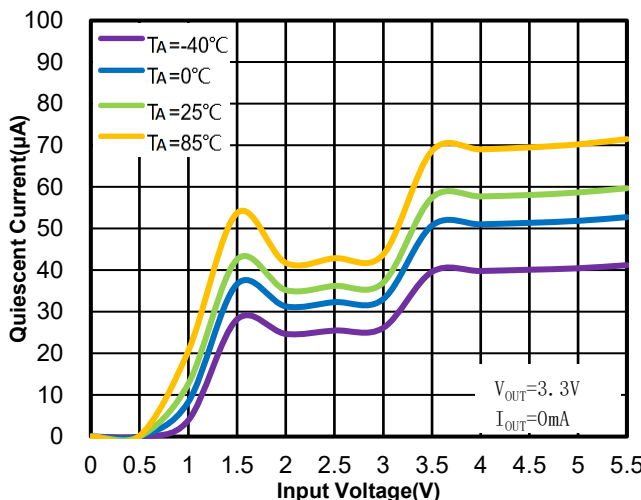
Figure 23. WR0512-33A20R
Quiescent Current vs. V_{IN} & Ambient Temperature
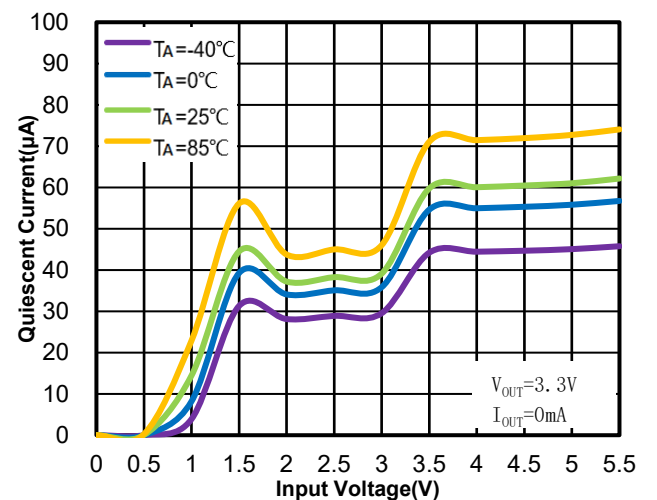
Figure 24. WR0512-33A50R
Quiescent Current vs. V_{IN} & Ambient Temperature

Typical Performance Characteristics (T_A= -40 to 85ºC, $V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=4.7\mu F$, unless otherwise noted)

Figure 25. WR0512-33A20R
Foldback Current Limit vs. I_{OUT} & Ambient Temperature
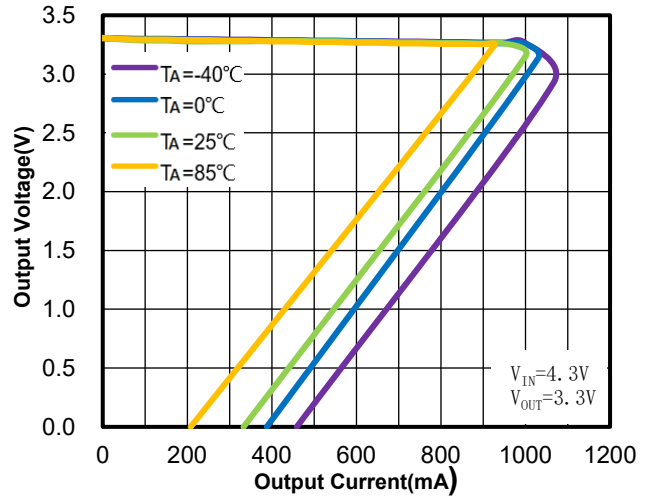
Figure 26. WR0512-33A50R
Foldback Current Limit vs. I_{OUT} & Ambient Temperature
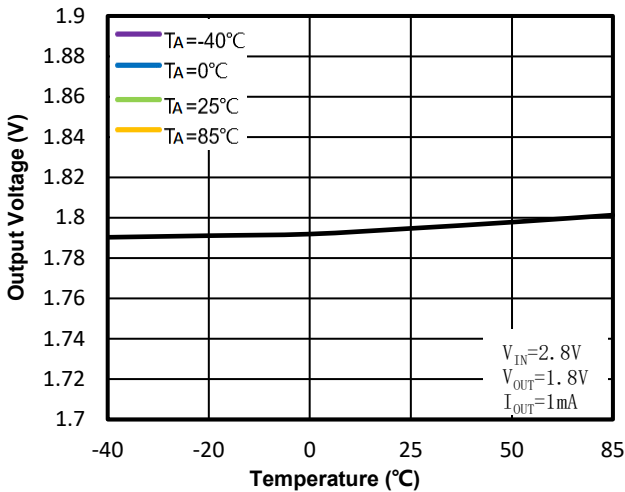
Figure 27. WR0512-18A20R
Output Voltage vs. Ambient Temperature
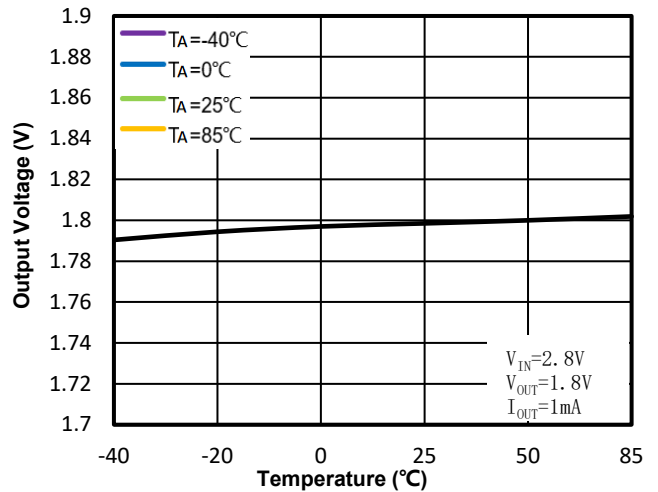
Figure 28. WR0512-18A50R
Output Voltage vs. Ambient Temperature
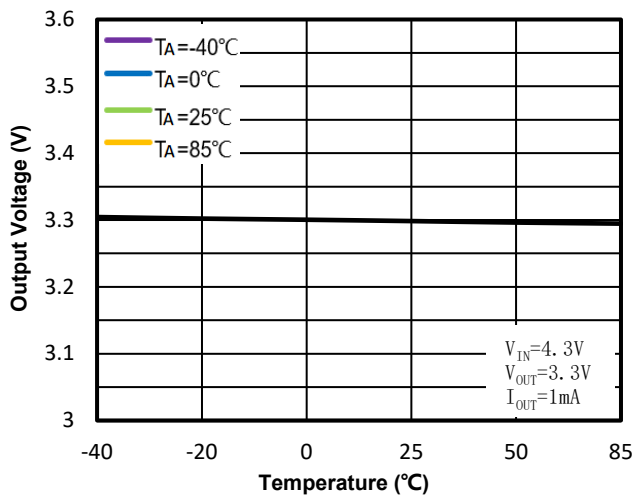
Figure 29. WR0512-33A20R
Output Voltage vs. Ambient Temperature
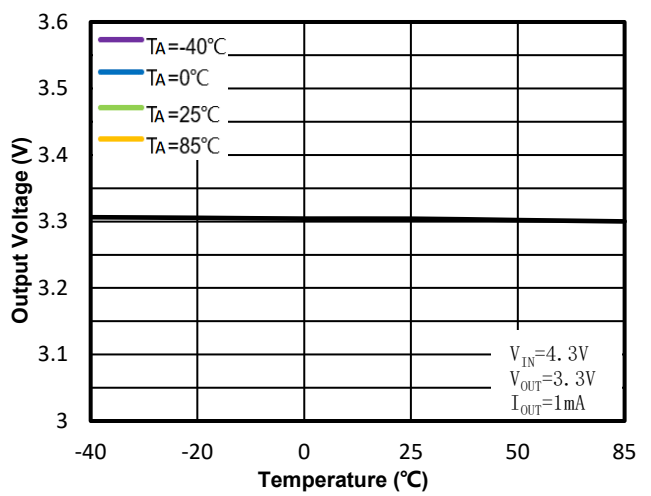
Figure 30. WR0512-33A50R
Output Voltage vs. Ambient Temperature

Typical Performance Characteristics (T$_A$= -40 to 85ºC, V$_{IN}$=V$_{OUT}$+1V, C$_{IN}$=C$_{OUT}$=4.7μF, unless otherwise noted)

V$_{IN}$=2.8V
V$_{OUT}$=1.8V
I$_{OUT}$=0mA

Figure 31. WR0512-18A20R
Quiescent Current vs. Ambient Temperature

V$_{IN}$=2.8V
V$_{OUT}$=1.8V
I$_{OUT}$=0mA
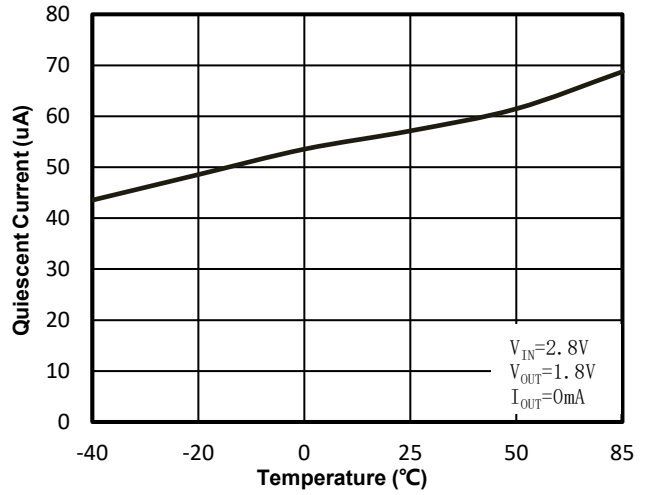
Figure 32. WR0512-18A50R
Quiescent Current vs. Ambient Temperature

V$_{IN}$=4.3V
V$_{OUT}$=3.3V
I$_{OUT}$=0mA
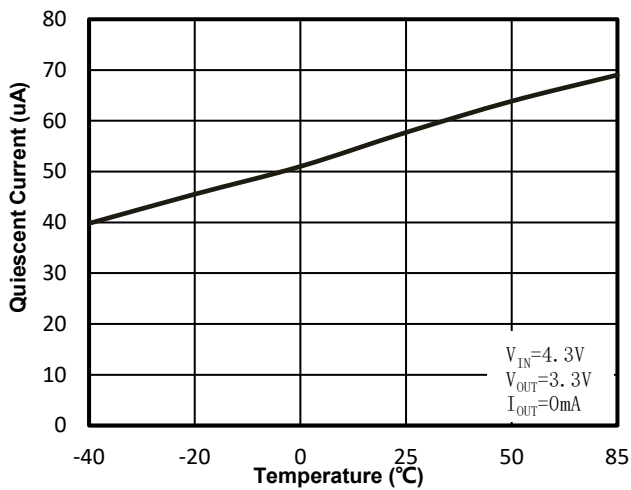
Figure 33. WR0512-33A20R
Quiescent Current vs. Ambient Temperature

V$_{IN}$=4.3V
V$_{OUT}$=3.3V
I$_{OUT}$=0mA
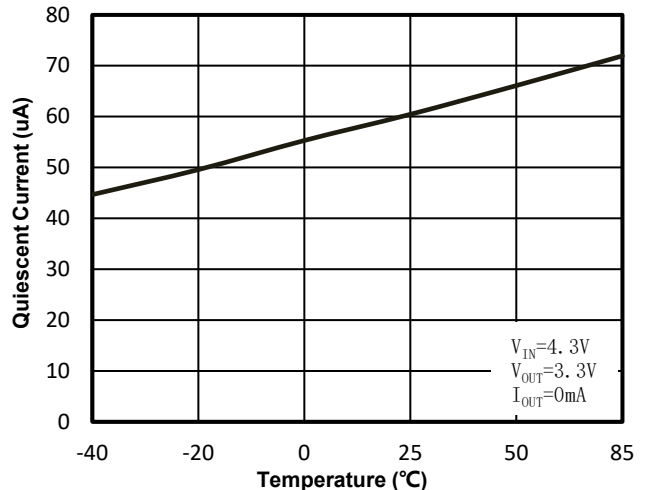
Figure 34. WR0512-33A50R
Quiescent Current vs. Ambient Temperature
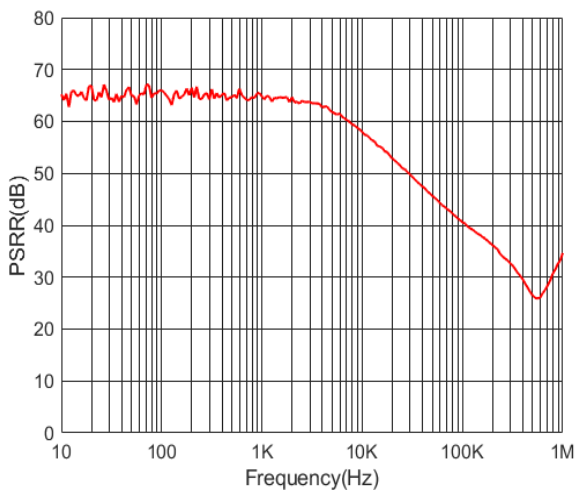
Figure 35. Power Supply Rejection Ratio vs. Frequency

Typical Performance Characteristics (T$_A$= -40 to 85ºC, V$_{IN}$=V$_{OUT}$+1V, C$_{IN}$=C$_{OUT}$=4.7μF, unless otherwise noted)

V$_{IN}$=2.8V
V$_{OUT}$=1.8V
I$_{OUT}$=10mA
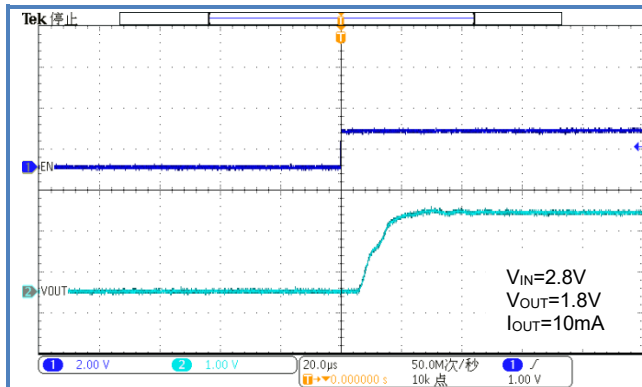
Figure 36.Soft Start from EN

V$_{IN}$=2.8V
V$_{OUT}$=1.8V
I$_{OUT}$=10mA

Figure 37.EN Shutdown

V$_{IN}$=4.3V
V$_{OUT}$=3.3V
I$_{OUT}$=10mA
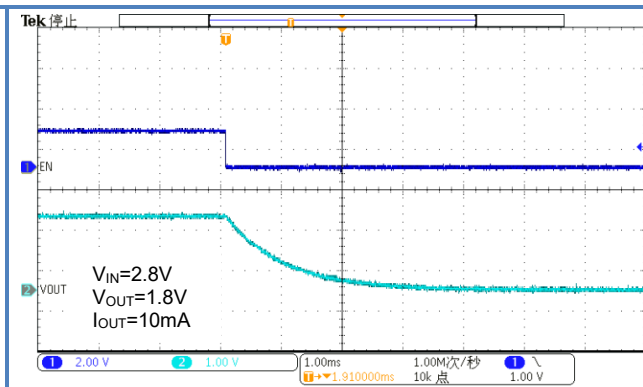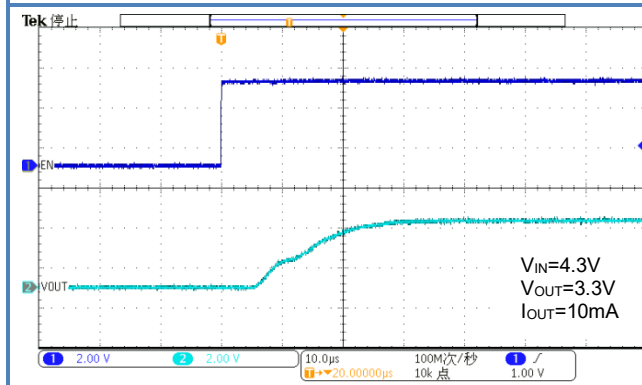
Figure 38.Soft Start from EN

V$_{IN}$=4.3V
V$_{OUT}$=3.3V
I$_{OUT}$=10mA

Figure 39.EN Shutdown

V$_{IN}$=2.8V to 5.5V
V$_{OUT}$=1.8V
I$_{OUT}$＝1mA
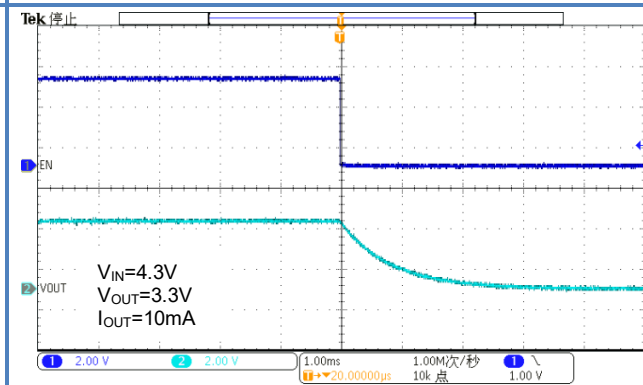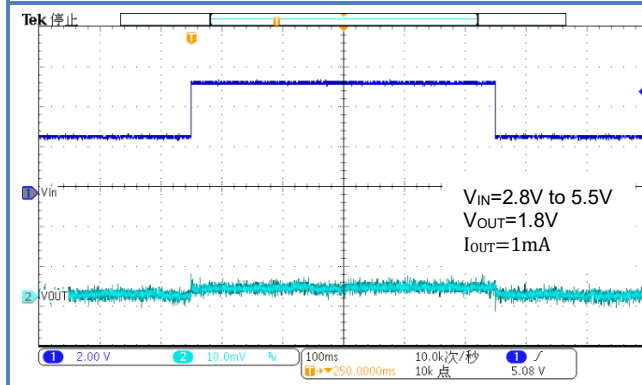
Figure 40.Line Transient

V$_{IN}$=2.8V
V$_{OUT}$=1.8V
I$_{OUT}$=1mA to 300mA
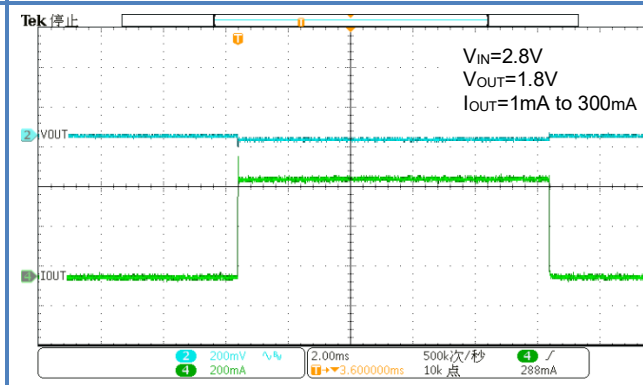
Figure 41.Load Transient

V$_{IN}$=4.3V to 5.5V
V$_{OUT}$=3.3V
I$_{OUT}$＝1mA
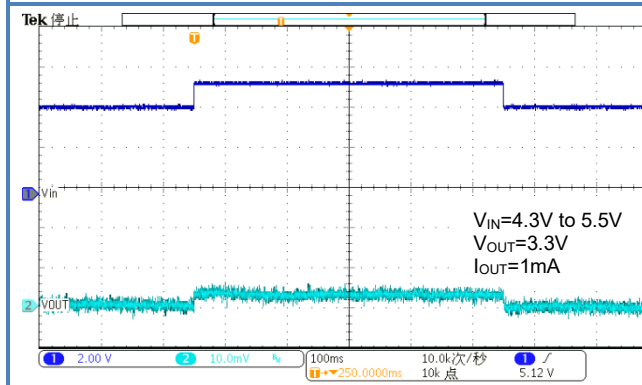
Figure 42. Line Transient

V$_{IN}$=4.3V
V$_{OUT}$=3.3V
I$_{OUT}$=1mA to 300mA
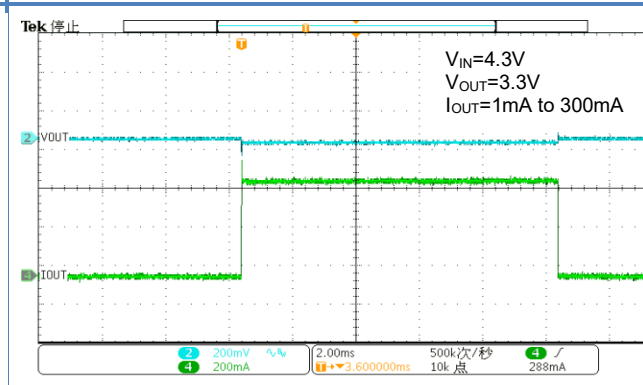
Figure 43.Load Transient

11. Function Description

11.1 Overview

The WR0512 series are ultra-low dropout, low quiescent current, high PSRR CMOS LDO. The dropout voltage is 130mV (Typ.) at 500mA load current. Using CMOS construction, the quiescent current consumed by the WR0512 is typically 60μA over the entire input voltage range, making it attractive for consumer, networking applications that demand high output current. The WR0512 series are available in wide output voltage range version from 1.2V to 3.3V with 0.1V step.

11.2 Block Diagram
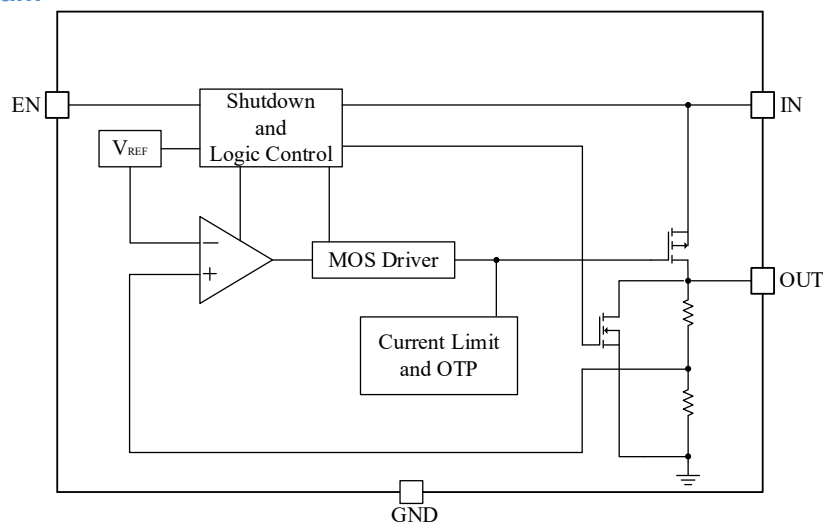
11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR0512 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Enable (EN)

The WR0512 enable pin contains a small pull-up current source, typically 0.1μA. When the input voltage of the enable pin is higher than the high enable voltage threshold, the device outputs normally. When the input voltage of the enable pin is lower than the low input voltage threshold of the EN pin, the device outputs shutdown.

If you do not need to control the output voltage independently, connect the enable pin to the input of the device.

11.3.3 Dropout Voltage (V_{DO})

WR0512 is a ultra-low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the V_{IN}-V_{OUT} at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the $R_{DS (ON)}$ of the pass-FET.

The $R_{DS (ON)}$ is calculated as follows:

$$R_{DS (ON)} = V_{DO}/I_{RATED}$$

11.3.4 Power Supply Rejection Ratio (PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is

$$PSRR = 20log(Ripple(in) / Ripple(out))$$

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0512 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.5 Noise

LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics; external noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input; internal noise is always present at the output of the LDO.

In practice, minimising noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR0512 has a low noise reference, high PSRR to ensure that output noise is reduced during normal operation.

11.3.6 Output Soft-Start

Soft-start is the ramping characteristic of the output voltage during the LDO turn-on period after EN and UVLO have exceeded the threshold, preventing the damage caused by output voltage overshoot to the subordinate circuits and enabling effective protection of the secondary circuits. The soft-start ramp can be programmed using a noise reduction capacitor ($C_{NR/SS}$). A larger value of noise reduction capacitor will reduce noise, but will also result in a slower output turn-on ramp. Higher currents allow a reasonable start-up time to be maintained with a larger noise reduction capacitor.
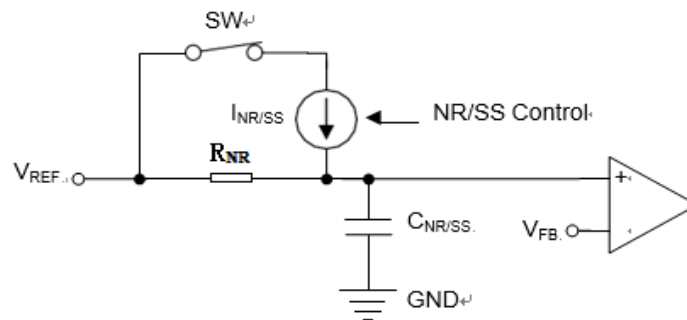
Soft-Start Circuit

11.3.7 Foldback Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{MAX}, and the output voltage will be reduced to $I_{MAX}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX}. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to $I_{FB}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR0512 uses a foldback current limiting mode where the final current is clamped to around 400mA, thus providing good protection to the device.

More information on current limiting can be found in Electrical Characteristics *Figure 25* to *Figure 26*.

11.3.8 Thermal Protection

The WR0512 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 165°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 135°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0512's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0512 into a thermal shutdown state will reduce the reliability of the device.

For reliable operation, limit the junction temperature to a maximum of 125°C. The thermal margin in a given layout is to be estimated. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition of the application.

11.4   Functional Mode Of The Device

The device has three modes: normal, dropout, and disabled modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal	$5.5V \geq V_{IN} \geq V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{UVLO} \leq V_{IN} \leq V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(nom)} + V_{DO}$) and is less than 5.5V.

2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.

3. The output current is less than the current limit ($I_{OUT} < I_{CL}$).

4. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

11.4.3 Disabled

The WR0512 can be turned off by forcing the enable pin low, typically with an enable voltage below 0.4V, at which point the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground through an internal resistor from output to ground.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0512 is a linear voltage regulator with an input voltage of 2.5V to 5.5 V and an output voltage of 1.2V to 3.3 V. The accuracy is 3% for output voltages up to 1.5 V and 2% for output voltages greater than 1.5 V. The maximum output current is 500 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Start-Up

12.1.1.1 Enable (EN)

The WR0512 can determine the output of the device through the EN input voltage, EN is higher than the voltage threshold to turn on, in order to prevent the device from turning off when the input voltage drops during the turn-on period, EN has a certain hysteresis. WR0512 internal EN to IN has a pull-up resistor, the pull-up current is about 100nA, when EN floats default to high, if you do not need EN independent control, it is recommended to connect EN directly to IN. If you want to use the EN control, you need to give a control voltage to the EN side.

12.1.1.2 Automatic Discharge

The WR0512 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.1.3 Soft-Start

Soft start refers to the characteristic that the output voltage rises gradually as the EN voltage jumps from low to high. Reducing the output voltage rise rate reduces the inrush current that charges the output capacitor. The inrush current is the current entering the LDO during startup and consists of the load current, the current charging the output capacitor, and the ground pin current.

The inrush current can be estimated by the following equation :

$$I_{OUT}(t) = (\frac{C_{OUT} \times dV_{OUT}(t)}{dt}) + (\frac{V_{OUT}(t)}{R_{LOAD}})$$

The WR0512 controls soft-start through an external capacitor (CNR/SS), which helps to reduce inrush current and reduce load transients on the input power bus, thus solving startup initialization problems that can result when powering FPGAs, DSPs, or other high-current loads.

12.1.2 Capacitor Recommendation

The WR0512 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good capacitance stability at different temperatures. WR0512 is designed to use ceramic capacitors of 1 μF or larger at the input and output. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device. Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacit-

or can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation (PD)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

PD can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage. The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators Ψ_{JT} or Ψ_{JB} are given in the thermal information table and can be used according to the following equation.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \times P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \times P_D$

Notes.
- P_D is the power dissipated.
- T_T is the temperature at the top center of the device package.
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.
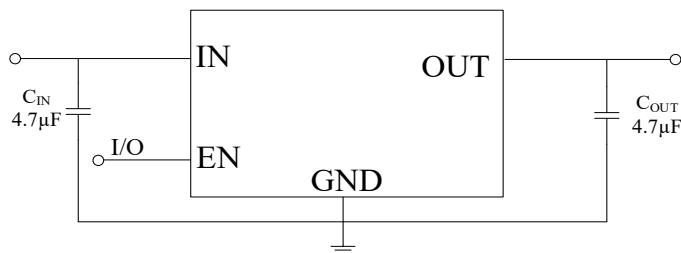
12.2 Typical Application

This section discusses the application of the WR0512 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic 1: V_{OUT} normally open, no control.
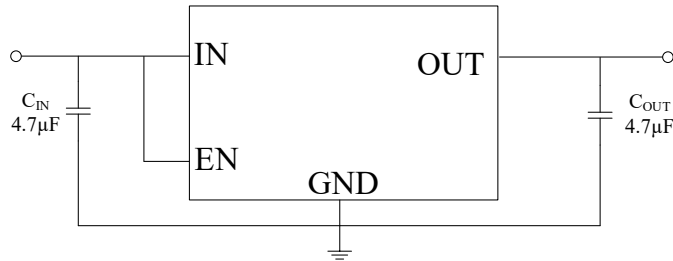
Circuit schematic 2: V_{OUT} control by external voltage to EN.

C_{IN} and C_{OUT} are to be selected with the recommended appropriate capacitance. 4.7μF ceramic capacitors are selected for both C_{IN} and C_{OUT} to help balance the charge needed to charge the output capacitor during startup, thus reducing the input voltage drop.

13. Power supply recommendation

The WR0512 has a V_{IN} range of between 2.5V and 5.5 V and an input capacitance of 4.7μF. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

Layout Example：
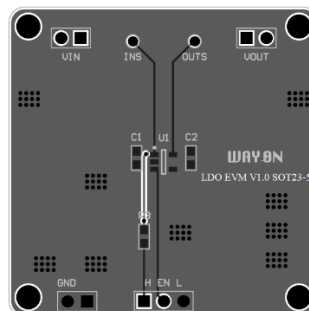
15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
WR0512	SOT23-3	WAYON LDO EVM V1.0 -SOT23-3
	SOT23-5	WAYON LDO EVM V1.0 -SOT23-5
	SOT89-3	WAYON LDO EVM V1.0 -SOT89-3
	SOT89-3L	WAYON LDO EVM V1.0 -SOT89-3L

16. Naming conventions

WR AA BB-CC DDD E

WR: WAYON Regulator

AA: 01/03/05/06 - Output Current, 100/300/500/600mA

BB: Serial number

CC: Output Voltage -Output Voltage

DDD: A20/21-Package, SOT89-3/3L

A30-Package, SOT23-3

A50-Package, SOT23-5

E: R-Reel & T-tube

17. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

18. Package Information

SOT 23-3
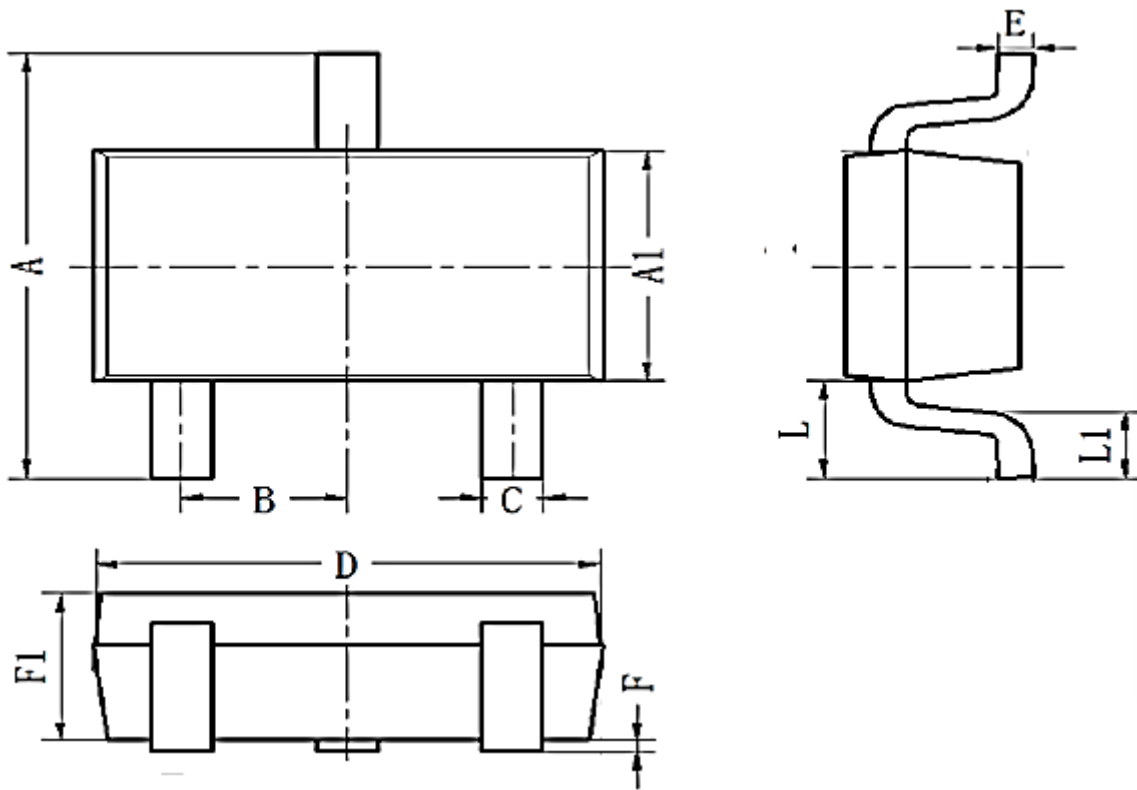
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	2.60	2.80	3.00
A1	1.50	1.60	1.70
B	0.95BSC		
C	0.25	0.40	0.50
D	2.82	2.92	3.02
E	0.10	0.15	0.20
L	0.59REF		
L1	0.30	0.45	0.60
F1	0.90	1.10	1.30
F	0.00	0.08	0.15

SOT 23-5
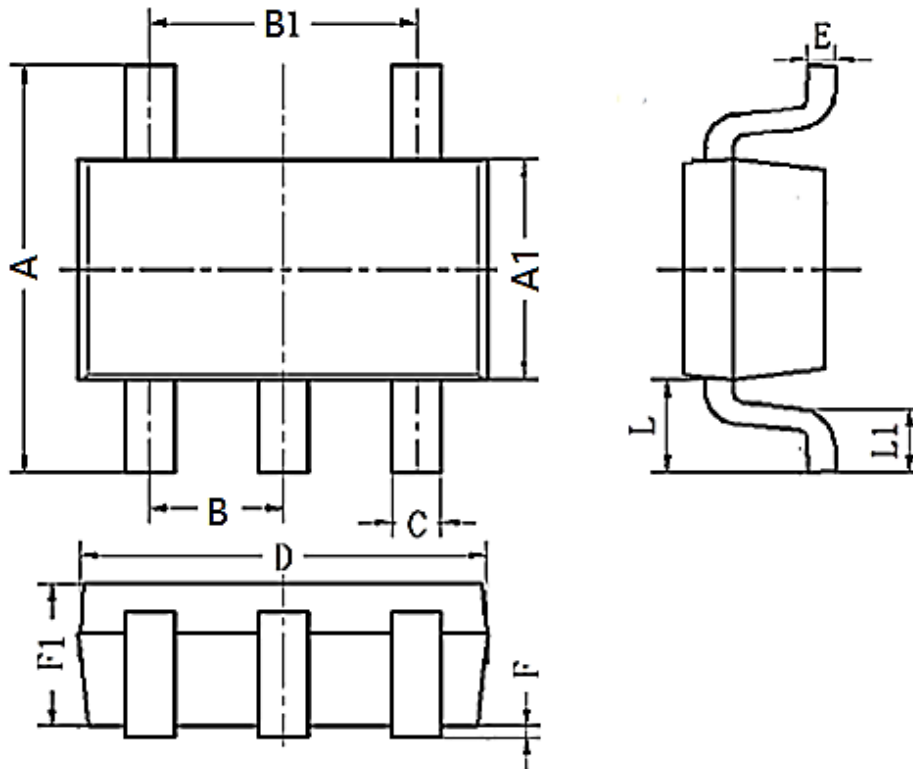
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	2.60	2.80	3.00
A1	1.50	1.60	1.70
B	0.95BSC		
B1	1.90BSC		
C	0.25	0.40	0.50
D	2.82	2.92	3.02
E	0.10	0.15	0.20
F	0.00	0.08	0.15
L	0.59REF		
F1	0.90	1.10	1.30
L1	0.30	0.45	0.60

SOT89-3/L
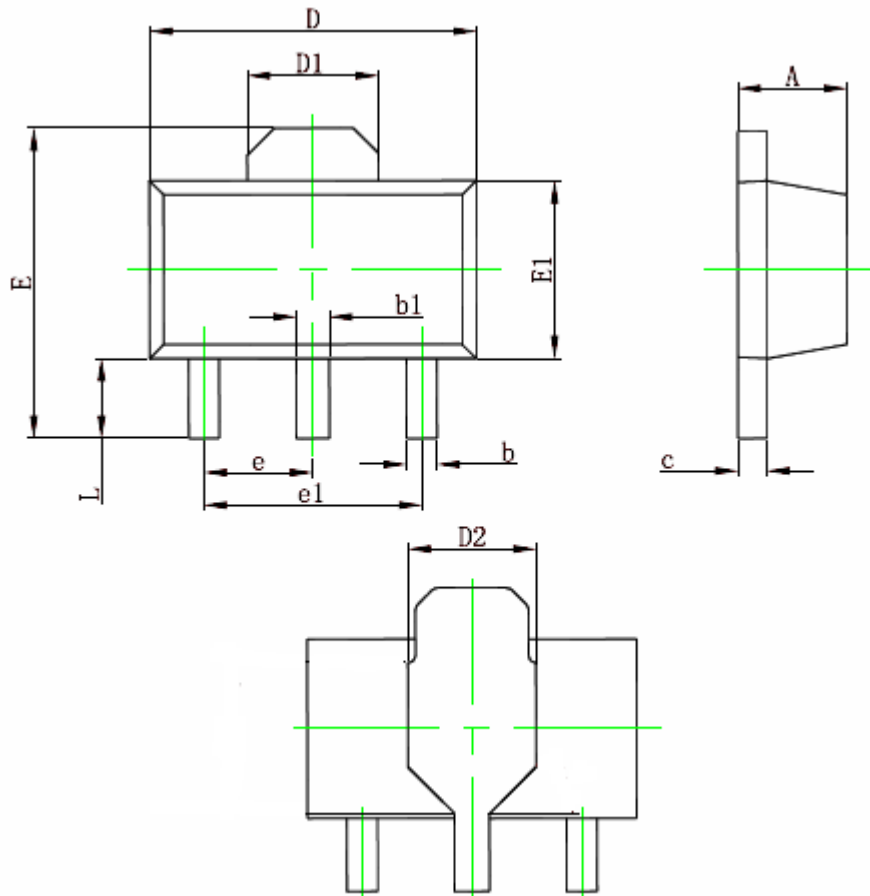
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.4	1.5	1.6
b	0.320	0.420	0.520
b1	0.380	0.480	0.580
c	0.350	0.405	0.460
D	4.400	4.500	4.600
D1	1.65REF		
D2	1.700	1.950	2.200
E	3.940	4.120	4.300
E1	2.300	2.450	2.600
e	1.5BSC		
e1	3.00BSC		
L	0.800	1.000	1.200

19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0512-12A50R	1.2V	SOT23-5	3k/Reel	WR0512 12 XXXX
WR0512-15A50R	1.5V	SOT23-5	3k/Reel	WR0512 15 XXXX
WR0512-18A50R	1.8V	SOT23-5	3k/Reel	WR0512 18 XXXX
WR0512-20A50R	2.0V	SOT23-5	3k/Reel	WR0512 20 XXXX
WR0512-22A50R	2.2V	SOT23-5	3k/Reel	WR0512 22 XXXX
WR0512-25A50R	2.5V	SOT23-5	3k/Reel	WR0512 25 XXXX
WR0512-28A50R	2.8V	SOT23-5	3k/Reel	WR0512 28 XXXX
WR0512-30A50R	3.0V	SOT23-5	3k/Reel	WR0512 30 JXXXX
WR0512-33A50R	3.3V	SOT23-5	3k/Reel	WR0512 33 JXXXX
WR0512-12A20R	1.2V	SOT89-3	1k/Reel	WR0512 12 XXXX
WR0512-15A20R	1.5V	SOT89-3	1k/Reel	WR0512 15 JXXXX
WR0512-18A20R	1.8V	SOT89-3	1k/Reel	WR0512 18 XXXX
WR0512-20A20R	2.0V	SOT89-3	1k/Reel	WR0512 20 XXXX
WR0512-22A20R	2.2V	SOT89-3	1k/Reel	WR0512 22 XXXX
WR0512-25A20R	2.5V	SOT89-3	1k/Reel	WR0512 25 XXXX
WR0512-28A20R	2.8V	SOT89-3	1k/Reel	WR0512 28 XXXX
WR0512-30A20R	3.0V	SOT89-3	1k/Reel	WR0512 30 JXXXX
WR0512-33A20R	3.3V	SOT89-3	1k/Reel	WR0512 33 JXXXX
WR0512-12A21R	1.2V	SOT89-3L	1k/Reel	WR0512 12 XXXX
WR0512-15A21R	1.5V	SOT89-3L	1k/Reel	WR0512 15 XXXX
WR0512-18A21R	1.8V	SOT89-3L	1k/Reel	WR0512 18 XXXX
WR0512-20A21R	2.0V	SOT89-3L	1k/Reel	WR0512 20 XXXX
WR0512-22A21R	2.2V	SOT89-3L	1k/Reel	WR0512 22 XXXX
WR0512-25A21R	2.5V	SOT89-3L	1k/Reel	WR0512 25 XXXX
WR0512-28A21R	2.8V	SOT89-3L	1k/Reel	WR0512 28 XXXX
WR0512-30A21R	3.0V	SOT89-3L	1k/Reel	WR0512 30 XXXX
WR0512-33A21R	3.3V	SOT89-3L	1k/Reel	WR0512 33 XXXX
WR0512-12A30R	1.2V	SOT23-3	3k/Reel	WR0512 12 XXXX
WR0512-15A30R	1.5V	SOT23-3	3k/Reel	WR0512 15 XXXX
WR0512-18A30R	1.8V	SOT23-3	3k/Reel	WR0512 18 XXXX

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0512-20A30R	2.0V	SOT23-3	3k/Reel	WR0512 20 XXXX
WR0512-22A30R	2.2V	SOT23-3	3k/Reel	WR0512 22 XXXX
WR0512-25A30R	2.5V	SOT23-3	3k/Reel	WR0512 25 XXXX
WR0512-28A30R	2.8V	SOT23-3	3k/Reel	WR0512 28 XXXX
WR0512-30A30R	3.0V	SOT23-3	3k/Reel	WR0512 30 JXXXX
WR0512-33A30R	3.3V	SOT23-3	3k/Reel	WR0512 33 XXXX

* XXXX is variable. The chip is universal whether the marking has j or not.

STATEMENTS

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

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