WR0337

18V Low I_Q, 300mA CMOS Low Dropout Regulator

1. General Description

The WR0337 series can provide 300mA output current and the maximum input voltage is 18V，the series is a high accuracy, low noise, high speed, low dropout CMOS Linear regulator with high ripple rejection. The devices offer a new level of cost-effective performance in the battery-powered equipments, such as RF applications and other systems requiring a quiet input voltage.

The WR0337 has the fold-back maximum short output current which depends on the output voltage. So the current limit functions both as a short circuit protection and as an output current limiter.

The WR0337 regulators are available in standard DFN1212-4L package. Standard products are Pb-free and Halogen-free.

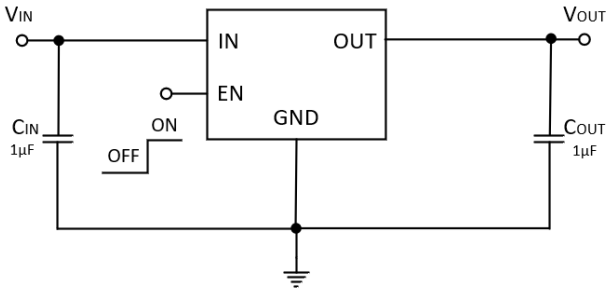
2. Applications

- MP3/MP4 Players
- Cellphones, radiophone, digital cameras
- Bluetooth, wireless handsets
- Others portable electronic device

3. Features

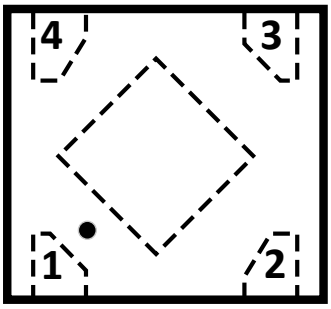
- Input Voltage: 2.5V~18V
- Output Voltage: 3.3V,5V
- Output Current: 300mA
- PSRR: 75dB@1kHz
- Dropout Voltage: 170mV @ I_{OUT} = 100mA
- Shut-down Current: < 1μA
- Quiescent Current: 3.0μA Typ.
- Recommend Capacitor: 1μF

4. Typical Application



5. Pin Configuration

(Top View)



DFN1212-4L

6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTIONS
1	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically 1μF, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 270-Ω (typical) pull-down resistor prevents a charge from remaining on VOUT when the regulator shutdowns.
2	IN	I	Input voltage supply. Bypass with a typical 1μF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.
3	GND	-	Ground.
4	EN	-	LDO enable.

7. Absolute Maximum Ratings[1]

PARAMETER		RATING	UNIT
Input voltage range		-0.3 to 20	V
Output voltage range		-0.3 to 5	V
Maximum output current		400	mA
Thermal Resistance, θ_{JA}	DFN1212-4L	150	ºC/W
Junction Temperature		150	ºC
Lead Temperature Range		260	ºC
Storage Temperature Range		-40 to 125	ºC
ESD Susceptibility	HBM	±4000	V

NOTE1: Greater than these given values, the device will be damaged.
NOTE2: The maximum current that can be output, but not guaranteed to work properly.

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Operating Supply voltage	2.5 to 18	V
Nominal output voltage range	3.3, 5	V
Output current	0 to 300	mA
Input capacitor	1	μF
Output capacitor	1	μF
Operating Temperature Range	-40 to 85	ºC

9. Electrical Characteristics ($V_{IN}=V_{OUT(NOM)}+1V$, $C_{IN}=C_{OUT}=1\mu F$, Full= -40℃ to 85℃, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage Range	V_{OUT} ≤1.5V, V_{IN}=2.5V, I_{OUT}=1mA,Full	0.97 V_{OUT}	V_{OUT}	1.03 V_{OUT}	V
		V_{OUT} > 1.5V, I_{OUT}=1mA,Full	0.98 V_{OUT}	V_{OUT}	1.02 V_{OUT}	
V_{DO}	Dropout Voltage[1]	V_{OUT}=3.3V, I_{OUT}=100mA,T_A=25℃		170		mV
		V_{OUT}=3.3V, I_{OUT}=200mA,T_A=25℃		370		
		V_{OUT}=3.3V, I_{OUT}=300mA,T_A=25℃		670		
I_{OUT}	Maximum Output Current[2]	V_{EN}=V_{IN} ,Full	300			mA
LNR	Line Regulation	V_{IN}=2.5~18V, I_{OUT}=1mA,Full		0.01	0.3	%/V
LDR	Load Regulation	V_{OUT}=3.3V, I_{OUT}=1~300mA,Full		20		mV
I_Q	Quiescent Current	V_{OUT}=3.3V, I_{OUT}=0mA,Full		3.0	5	μA
I_{SHORT}	Short Current	V_{OUT} Short to GND ,Full		90		mA
$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	Output Voltage Ambient Temperature Coefficient	I_{OUT}=10mA ,Full		50		ppm/ºC
PSRR	Power Supply Ripple Rejection	V_{IN}=(V_{OUT}+1V) $_{DC}$+0.5V_{P-P} f=1kHz, I_{OUT}=50mA, @V_{OUT}=3.3V ,T_A=25℃		75		dB
		V_{IN}=(V_{OUT}+1V) $_{DC}$+0.5V_{P-P} f=10kHz, I_{OUT}=50mA, @V_{OUT}=3.3V ,T_A=25℃		55		
V_{NO}	Output Noise Voltage	10Hz to 100kHz, C_{OUT}=1μF, I_{OUT}=10mA, T_A=25℃		27* V_{OUT}		μV_{RMS}
T_{SD}	Thermal Shutdown Threshold			150		ºC
ΔT_{SD}	Thermal Shutdown Hysteresis			15		ºC

Note1: The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is $V_{OUT(NOM)}$ * 98%.

Note2: Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN} < V_{OUT} + V_{DROP}.

Note3: The Load regulation is measured using pulse techniques with duty cycle < 5%.

10. Typical Performance Characteristics (T_A = -40°C to 85°C, V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

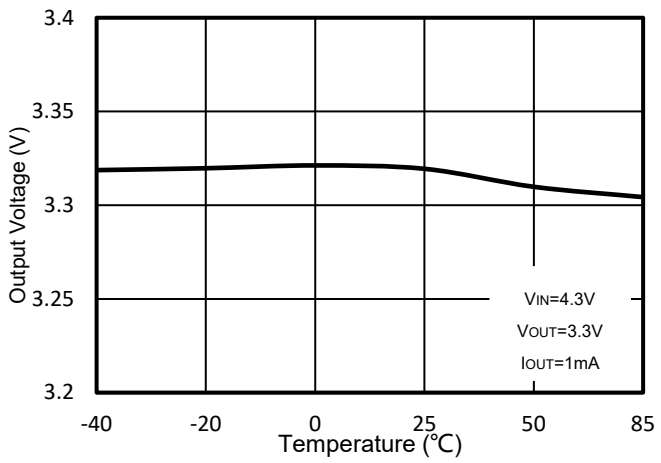


Figure 1. WR0337-33F14R
Output Voltage vs. Ambient Temperature

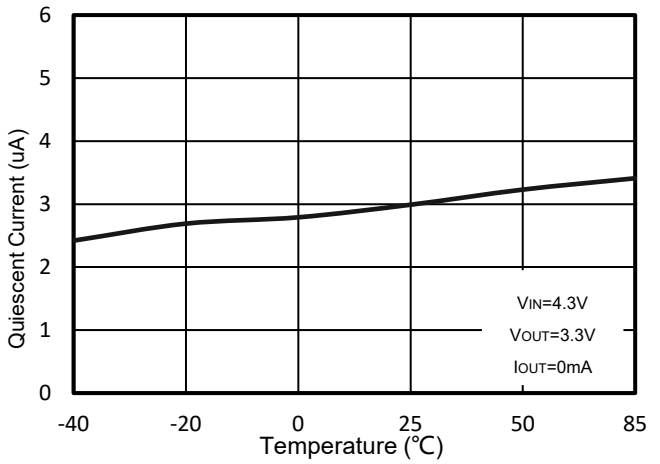


Figure 2. WR0337-33F14R
Quiescent Current vs. Ambient Temperature

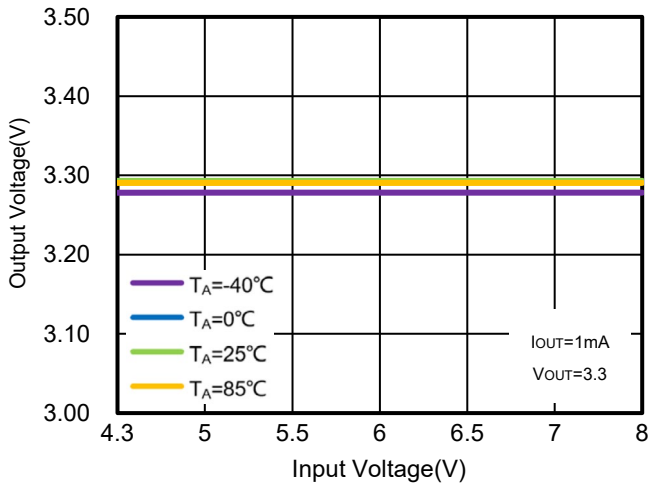


Figure 3. WR0337-33F14R
Regulation vs. V_{IN} (Line Regulation) & Ambient Temperature

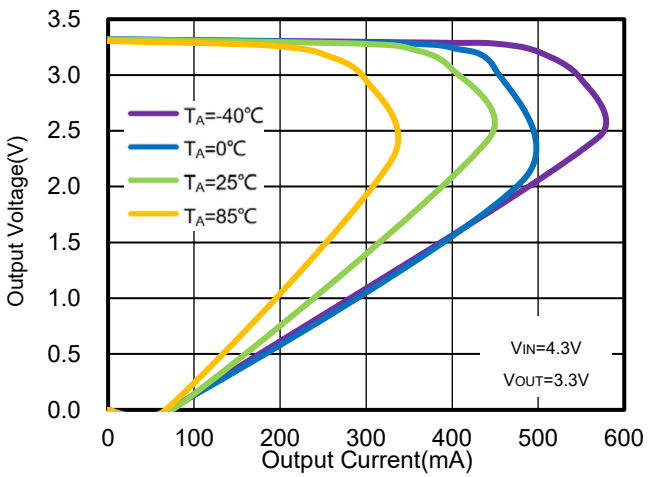


Figure 4. WR0337-33F14R
Foldback Current Limit vs. I_{OUT} & Ambient Temperature

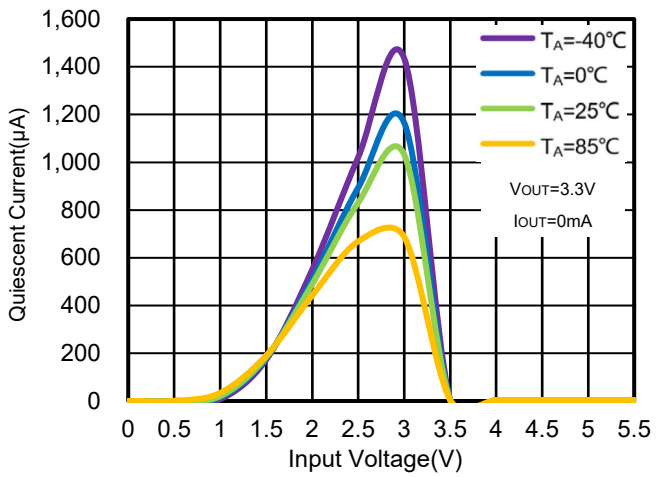


Figure 5. WR0337-33F14R
Quiescent Current vs. V_{IN} & Ambient Temperature

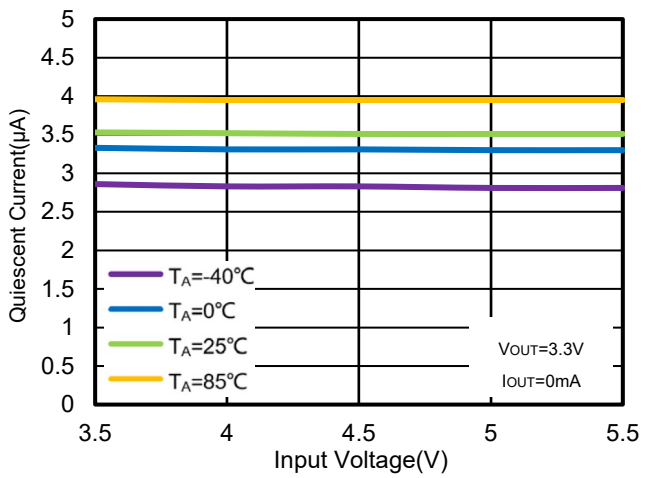


Figure 6. WR0337-33F14R
Quiescent Current vs. V_{IN} & Ambient Temperature

Typical Performance Characteristics (T_A = 25°C, V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

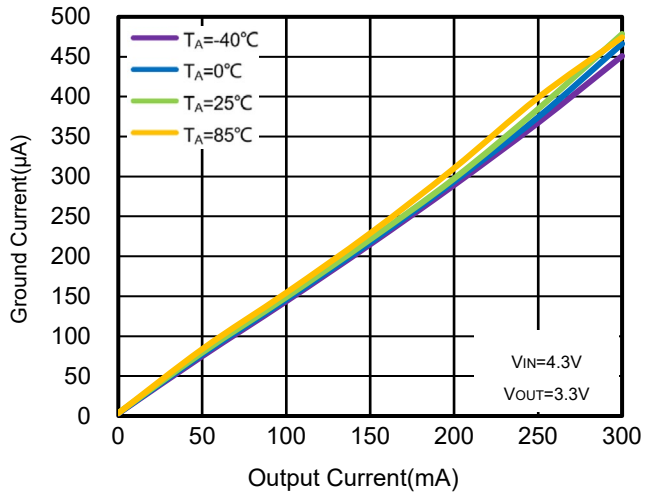


Figure 7. WR0337-33F14R
Ground Pin Current vs. I_{OUT} & Ambient Temperature

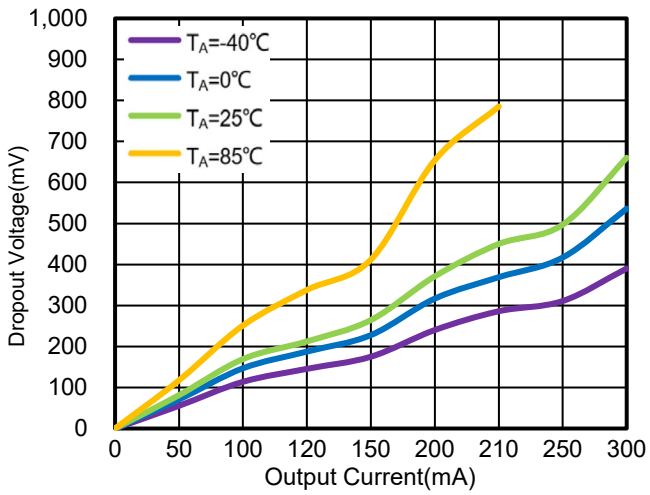


Figure 8. WR0337-33F14R
Dropout Voltage vs. I_{OUT} & Ambient Temperature

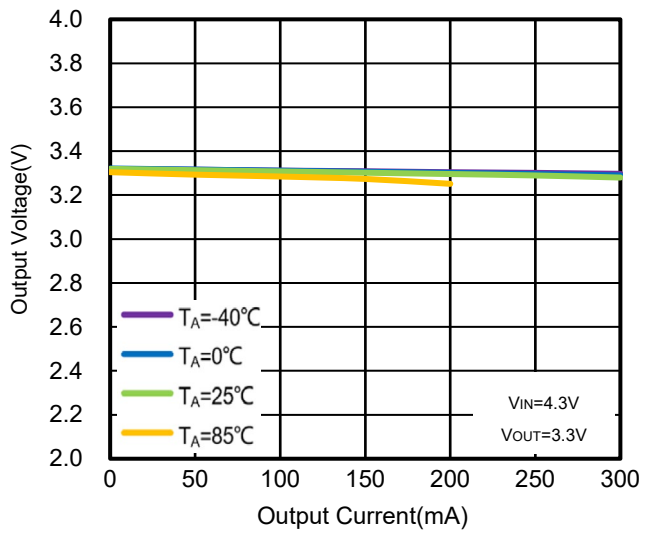


Figure 9. WR0337-33F14R
Output Voltage vs. I_{OUT} & Ambient Temperature

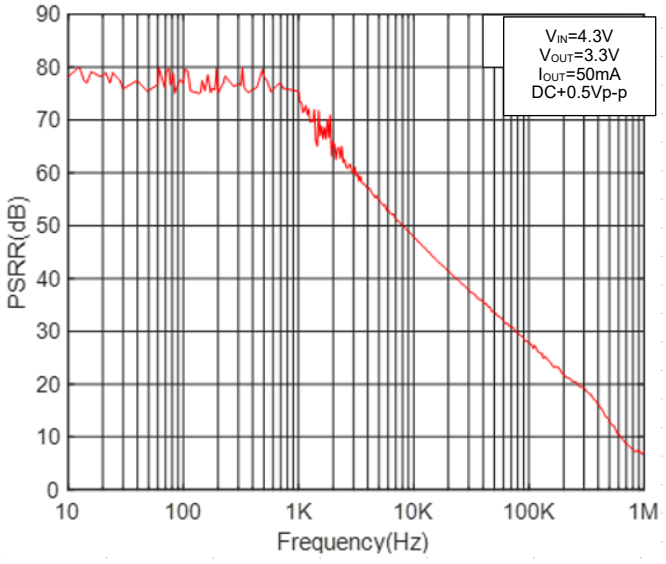


Figure 10. WR0337-33F14R
Power Supply Rejection Ratio vs. Frequency

Typical Performance Characteristics (T_A = 25°C, V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

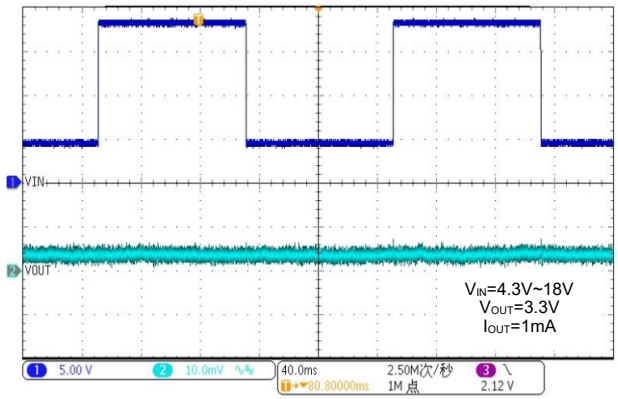


Figure 11. WR0337-33F14R
Line Transient

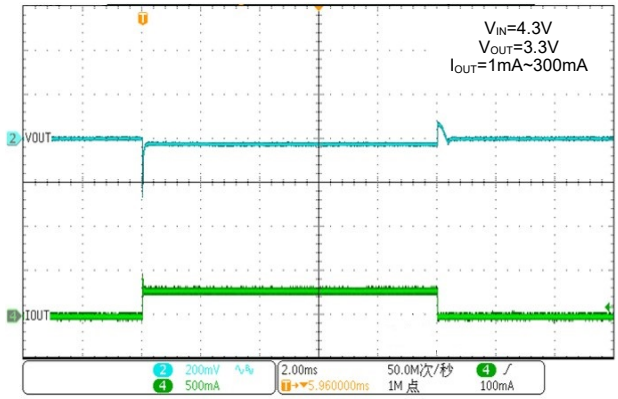


Figure 12. WR0337-33F14R
Load Transient

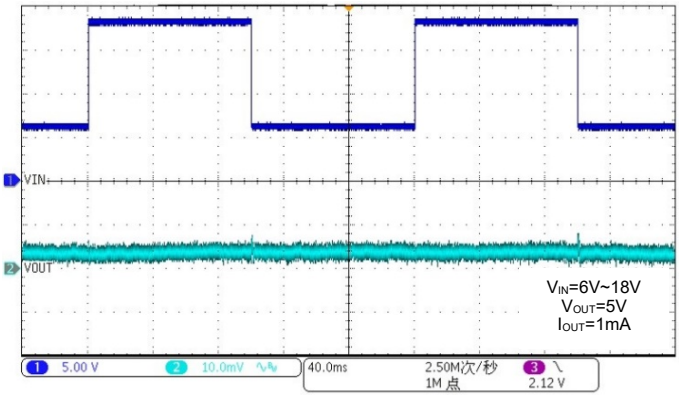


Figure 13. WR0337-50F14R
Line Transient

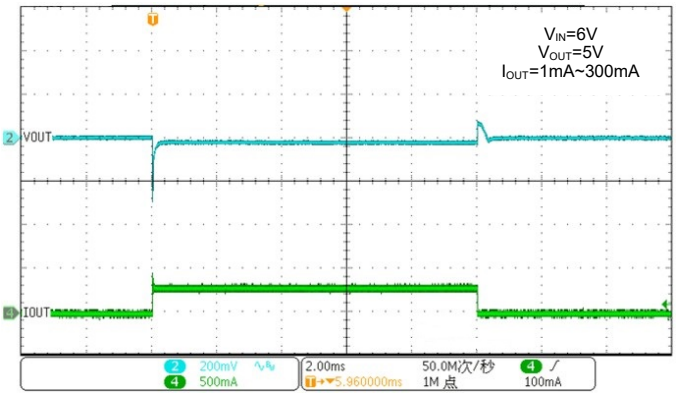


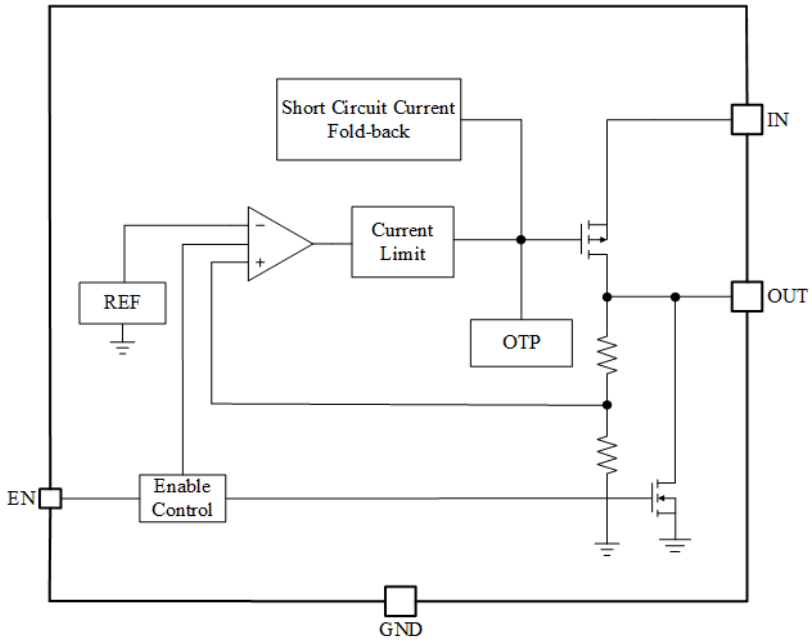
Figure 14. WR0337-50F14R
Load Transient

11. Function Description

11.1 Overview

The WR0337 is a low quiescent current regulator capable of providing 300 mA. With a wide input voltage range, up to 18V, the device also features a high PSRR, low dropout voltage and a very small package for space constrained applications. The WR0337 is designed to be used in a variety of applications.

11.2 Block Diagram



11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR0337 has an output voltage accuracy of 2%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Dropout Voltage (V_{DO})

WR0337 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the V_{IN}-V_{OUT} at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the $R_{DS\ (ON)}$ of the pass-FET. The $R_{DS\ (ON)}$ is calculated as follows:

$$R_{DS\ (ON)}=V_{DO}/I_{RATED}$$

11.3.3 Power Supply Rejection Ratio(PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources.

The basic calculation formula is:

PSRR = 20log(Ripple(in) / Ripple(out))

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0337 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.4 Noise

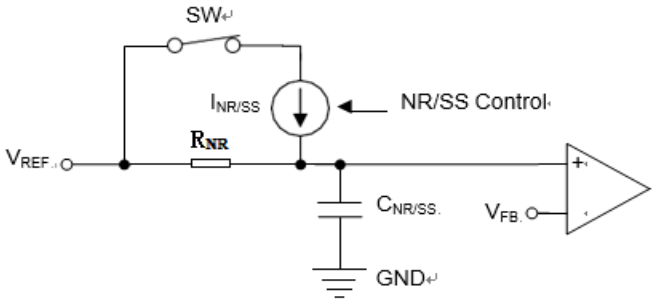
LDO noise can be divided into two main categories: internal noise and external noise. Internal noise is the noise generated inside the electronics. External noise is the noise transmitted from outside the circuit to the circuit. The error amplifier determines the PSRR of the LDO and therefore its ability to suppress external noise at the input. Internal noise is always present at the output of the LDO.

In practice, minimizing noise from the power supply is critical to system performance. In test and measurement systems, small fluctuations in power supply noise can alter the instantaneous measurement accuracy.

The WR0337 has a low noise reference, high PSRR to ensure that output noise is reduced during normal operation.

11.3.5 Output Soft-Start

Soft-start is the ramping characteristic of the output voltage during the LDO turn-on period after UVLO have exceeded the threshold, preventing the damage caused by output voltage overshoot to the subordinate circuits and enabling effective protection of the secondary circuits. The soft-start ramp can be programmed using a noise reduction capacitor ($C_{NR/SS}$). A larger value of noise reduction capacitor will reduce noise, but will also result in a slower output turn-on ramp. Higher currents allow a reasonable start-up time to be maintained with a larger noise reduction capacitor.



Soft-Start Circuit

11.3.6 Foldback Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX}, and when an overload or short circuit occurs, the output current will be maintained at I_{MAX}, and the output voltage will be reduced to $I_{MAX}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX}. The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to $I_{FB}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

The WR0337 uses a foldback current limiting mode where the final current is clamped to around 90mA, thus providing good protection to the device.

More information on current limiting can be found in Typical Performance Characteristics *Figure 4*.

11.3.8 Thermal Protection

The WR0337 contains a thermal shutdown protection circuit that implements the required switching gate circuit function through a thermal switch integrated inside the chip. The output current is turned off when the heat in the LDO is too high. Thermal shutdown occurs when the thermal junction temperature (T_J) of the energized crystal exceeds 150°C (typical). The thermal shutdown hysteresis ensures that the LDO resets (turns on) again when the temperature drops to 135°C (typical). The thermal time constant of the semiconductor chip is quite short, so when thermal shutdown is reached, the output turns on and off at a higher rate until the power dissipation is reduced.

The WR0337's internal protection circuitry is designed to prevent thermal overload conditions. This circuitry is not a substitute for a proper heat sink. Continuously putting the WR0337 into a thermal shutdown state will reduce the reliability of the device.

11.4 Functional Mode Of The Device

The device has two modes: normal and dropout modes of operation.

The operating conditions of each mode are listed in the table below.

Operating conditions of each mode

FUNCTIONAL MODE	CONDITIONS			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal	$18V>V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

11.4.1 Normal Mode

Normal operating mode requires that both of the following conditions are met.

1. The input voltage is greater than the rated output voltage plus the differential voltage ($V_{OUT(nom)} + V_{DO}$) and is less than 18V.
2. The enable voltage has previously exceeded the enable rise threshold voltage and has not fallen below the enable fall threshold.
3. The output current is less than the current limit ($I_{OUT} < I_{CL}$).
4. The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

11.4.2 Dropout Mode

If the input voltage is below the rated output voltage plus a specified dropout voltage, but all other conditions are met for normal operation, the device operates in the dropout state and the output voltage tracks the input voltage. Because the transient performance of the device is significantly reduced through the device being in the triode state, the output current is no longer controlled. Line or load transients during power down can result in large output voltage deviations.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0337 is a linear voltage regulator with an input voltage of 2.5 V to 18 V and an output voltage of 3.3 V and 5 V. The accuracy is 2% for output voltages. The maximum output current is 300 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Automatic Discharge

The WR0337 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.2 Capacitor Recommendation

The WR0337 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good

capacitance stability at different temperatures. WR0337 is designed to use ceramic capacitors of 1 μF or larger at the input and output. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device.

Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation(PD)

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

PD can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators Ψ_{JT} or Ψ_{JB} are given in the thermal information table and can be used according to the following equation:

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

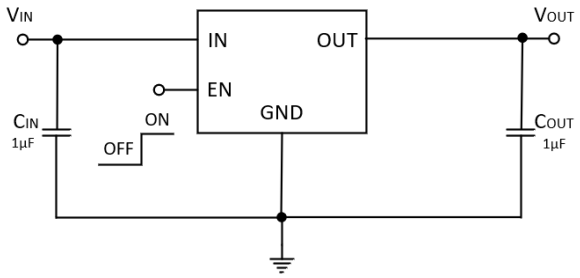
Notes:

- P_D is the power dissipated.
- T_T is the temperature at the top center of the device package.
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.

12.2 Typical Application

This section discusses the application of the WR0337 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic:



C_{IN} and C_{OUT} are to be selected with the recommended appropriate capacitance. 1μF ceramic capacitors are selected for both C_{IN} and C_{OUT} to help balance the charge needed to charge the output capacitor during startup, thus reducing the input voltage drop.

13. Power Supply Recommendation

The WR0337 has a V_{IN} range of between 2.5 V and 18 V and an input capacitance of 1μF. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
WR0337	DFN1212-4L	WAYON LDO EVM V1.0 DFN1212-4L

16. Naming Conventions

WR AA BB-CC DDD E

WR: WAYON Regulator

AA: 01/03/05/06 - Output Current, 100/300/500/600mA

BB: Serial number

CC: Output Voltage/AD-Output Voltage, Adjustable Voltage

DDD: F14-Package, DFN1212-4L

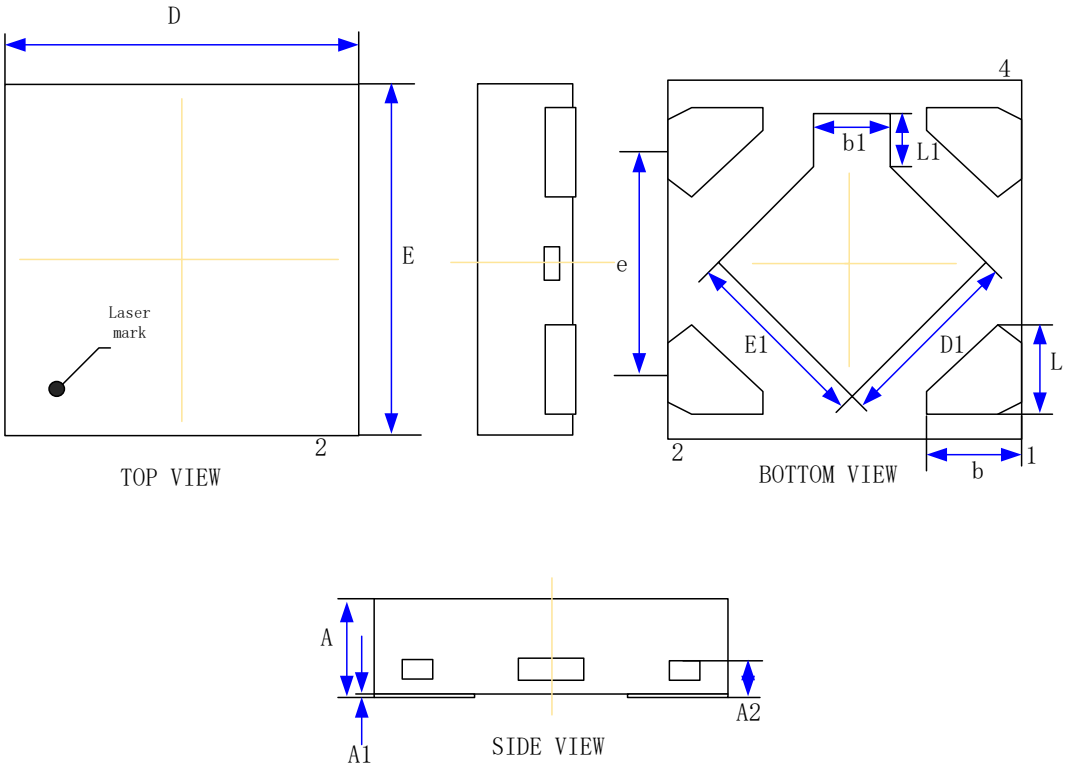
E: R-Reel & T-tube

17. Electrostatic Discharge Warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more *susceptible* to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

18. Package Information

DFN1212-4L



DFN1.2*1.2-4L

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
e	0.800BSC		
A2	0.127REF		
D	1.15	1.20	1.25
E	1.15	1.20	1.25
D1	0.58	0.63	0.68
E1	0.58	0.63	0.68
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
L	0.25	0.30	0.35
L1	0.13	0.18	0.23

19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0337-33F14R	3.3V	DFN1212-4L	3k/Reel	337 33
WR0337-50F14R	5.0V	DFN1212-4L	3k/Reel	337 50

*XXXX is variable.

STATEMENTS

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

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