

General Descriptions

The WR0116 series is a set of low linear regulation, low load regulation, low power wide input voltage regulators implemented in CMOS technology, providing 100mA output current. The devices allow input voltages ranging from 3.5V to 30V, fixed version output voltages from 2.1V to 12V.

The devices can be used in a variety of applications with large dropout voltages and low quiescent currents. The low quiescent current makes this family of devices ideal for a wide range of battery operated handheld devices. The WR0116 has a foldback maximum output current and therefore the current limit functions as both a short circuit protection and an output current limiter to ensure the safety of the secondary circuit.

These devices offer a new cost-effective option for mobile phones, laptops and other portable devices.

The WR0116 is available in standard SOT23-3L. SOT23-5L and SOT89-3L packages. It has an operating ambient temperature range of -40°C to +125°C. The standard product is lead-free and halogen-free.

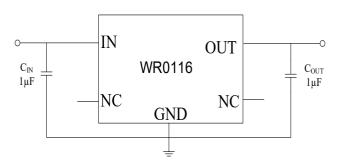
2. **Features**

- Ultra-low Quiescent Current
- Low Temperature Coefficient
- High Input Voltage (up to 30V)
- Output Current: 100mA
- Output Voltage Accuracy: ±3%
- Fixed Output Voltage Versions: 2.1V to 12V
- -40°C to +125°C Operating Temperature Range

3. Applications

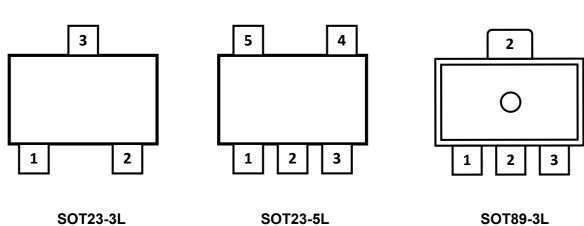
- Battery-Powered Equipment
- Communication Equipment
- Audio/Video Equipment

Typical Application



5. Pin Configuration

(Top View)



6. Pin Description

	PIN NUMBER		PIN NAME	I/O	PIN FUNCTIONS
SOT23-3L	SOT23-5L	SOT89-3L	T III TVAIII E	" "	T IN TONOTIONS
1	1	1	GND	-	Common ground.
2	2	2	IN	I	Input voltage supply. Bypass with a typical 1µF capacitor to GND. Place the input capacitor as close to the IN and GND pins of the device as possible.
3	3	3	OUT	0	Regulated output voltage. A low equivalent series resistance (ESR) capacitor, typically $1\mu F$, is required from OUT to ground for stability. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal $150-\Omega$ (typical) pull-down resistor prevents a charge from remaining on V_{OUT} when the regulator shutdowns.
-	4	-	NC	-	Not connect.
-	5	-	NC	-	Not connect

7. Absolute Maximum Ratings^[1]

100mA Ultra-low IQ, CMOS LDO

PARAM	METER	RATING	UNIT
Input volt	age range	-0.3 to 33	v
Output vol	tage range	-0.3 to V _{IN}	V
Maximum o	utput current	150 ^[2]	mA
	SOT23-3L	500	
Power Dissipation P _{D(MAX)} @T _A = 25°C	SOT23-5L	500	mW
PD(MAX)@1A - 25 C	SOT89-3L	625	
	SOT23-3L	250	
Thermal Resistance ^{[2] [4]}	SOT23-5L	250	°C/W
$R_{ heta JA}$	SOT89-3L	200	
Junction Temperature		150	
Lead Temperature (10s)		260	${\mathbb C}$
Storage Temperature Range		-55 to 150	
ESD Susceptibility	НВМ	±3000	V

NOTE1: Greater than these given values, the device will be damaged.

NOTE2: Measured on 2cm x 2cm 2-layer FR4 PCB board, 1 oz copper, no via holes on GND copper.

NOTE3: Power dissipation is calculate by $P_{D(MAX)}$ =(T_J -T_A) / $R_{\theta JA}.$

8. Recommended Operating Conditions

PARAMETER	RATING	UNIT
Input voltage range	3.5 to 30	
Nominal output voltage range	2.1 to 12	V
Output current	0 to 100	mA
Input capacitor	1	
Output capacitor	1	μF
Operating temperature range	-40 to 125	$^{\circ}$

WR0116

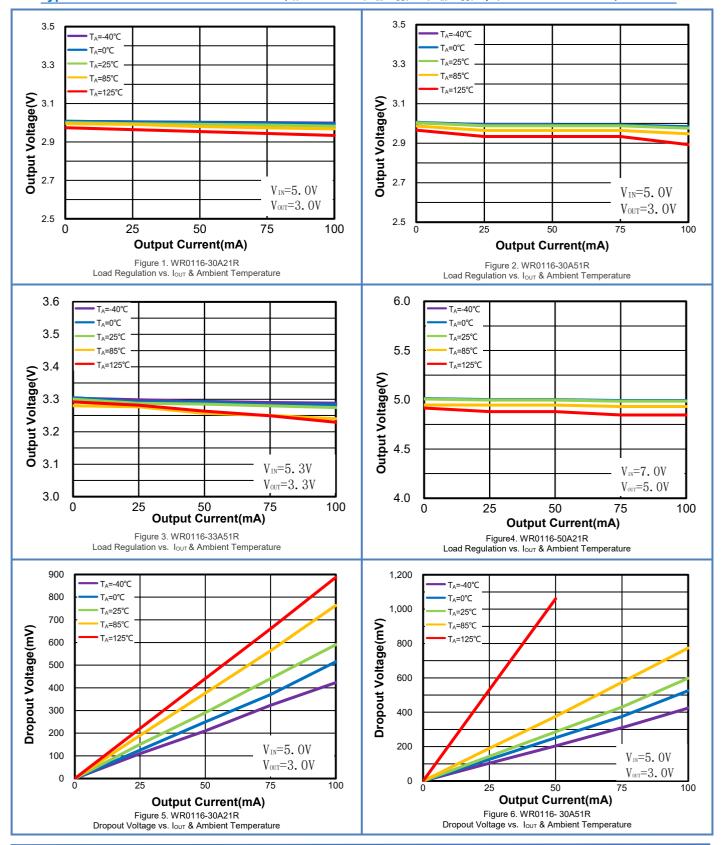
100mA Ultra-low IQ, CMOS LDO

9. Electrical Characteristics (V_{IN}=V_{OUT(NOMINAL)}+2V, C_{IN}=C_{OUT}=1µF, Full= -40 °C to 125 °C, unless otherwise noted)

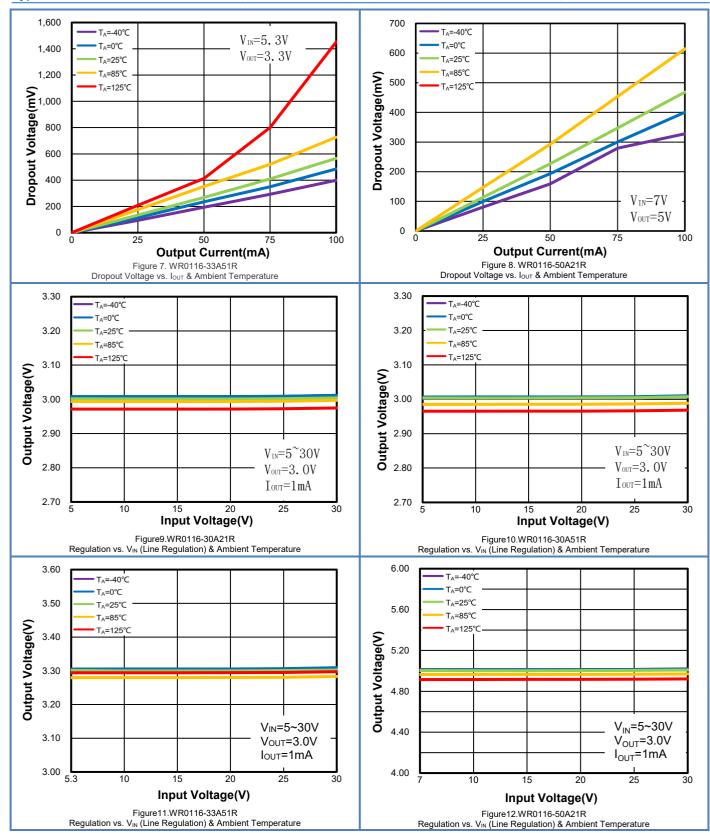
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{OUT}	Output Voltage Range	V _{IN} =V _{OUT} +2V, I _{OUT} =1mA, Full	0.97 V _{OUT}	V _{OUT}	1.03 V _{оит}	V	
		V _{OUT} =5.0V, I _{OUT} =50mA, Full		230		-	
.,	5 ()//// 1	V _{OUT} =3.3V, I _{OUT} =50mA, Full		270			
V_{DO}	Dropout Voltage ¹	V _{OUT} =3.0V, I _{OUT} =50mA, Full		290		mV	
		V _{OUT} =2.7V, I _{OUT} =50mA, Full		310			
I _{OUT}	Maximum output current in the accuracy range	V _{IN} =V _{OUT} +2V, Full	100			mA	
I _{SHORT}	Short Current	V_{OUT} Short to GND, Full		70		mA	
LNR	Line Regulation	V _{OUT} +1V≤V _{IN} ≤30V, I _{OUT} =1mA, Full			0.2	%/V	
LDR	Load Regulation ²	V _{IN} =V _{OUT} +2V, I _{OUT} =1~100mA, Full		25		mV	
lα	Quiescent Current	V _{IN} =V _{OUT} +2V,I _{OUT} =0mA , T _A =25°C		2.5	4.0	μA	
PSRR	Power Supply Ripple Rejection	$V_{IN}=(V_{OUT}+1V)_{DC}+0.5V_{P-P}$ f=1kHz, $I_{OUT}=10$ mA, @ $V_{OUT}=3.3V$, $T_{A}=25$ °C		37		dB	
$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	Output Voltage Temperature Coefficient	I _{OUT} =10mA, Full		100		ppm/°C	

Note1: The dropout voltage is defined as $(V_{IN}-V_{OUT})$, when V_{OUT} is $V_{OUT(NOM)}^*98\%$. **Note2:** The Load regulation is measured using pulse techniques with duty cycle < 5%.

10. Typical Performance Characteristics (T_A= -40 to 125°C, V_{IN}=V_{OUT}+2V, C_{IN}=C_{OUT}=1μF, unless otherwise noted)

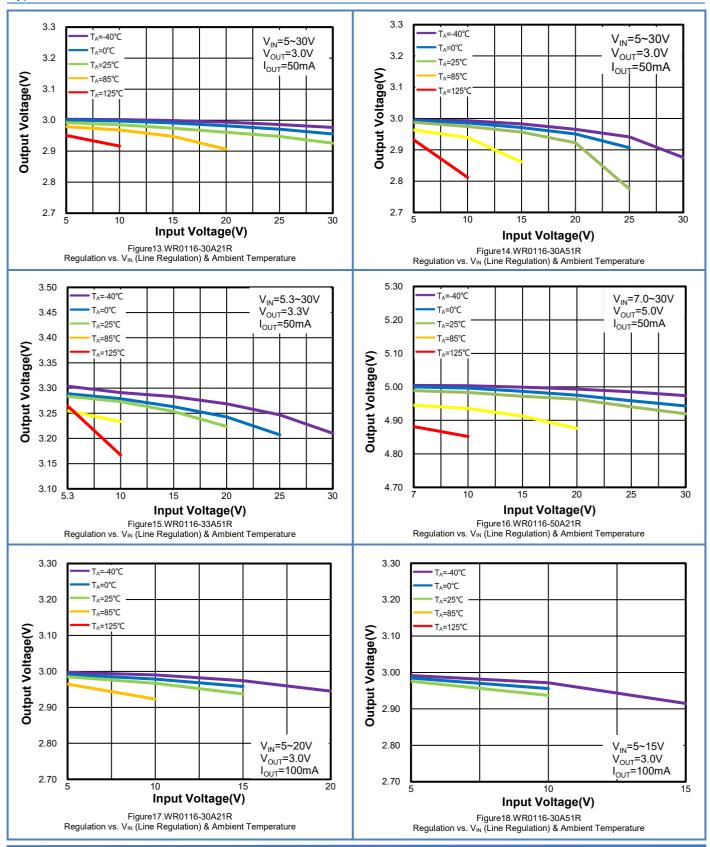


Typical Performance Characteristics (TA= -40 to 125°C, VIN=VOUT+2V, CIN=COUT=1µF, unless otherwise noted)



100mA Ultra-low IQ, CMOS LDO

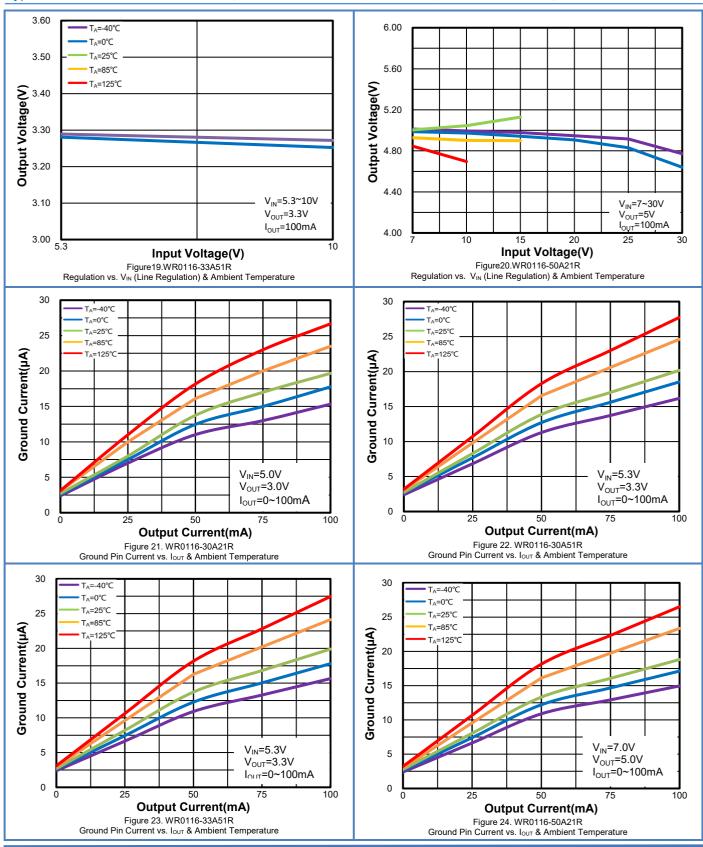
Typical Performance Characteristics (T_A= -40 to 125°C, V_{IN}=V_{OUT}+2V, C_{IN}=C_{OUT}=1µF, unless otherwise noted)



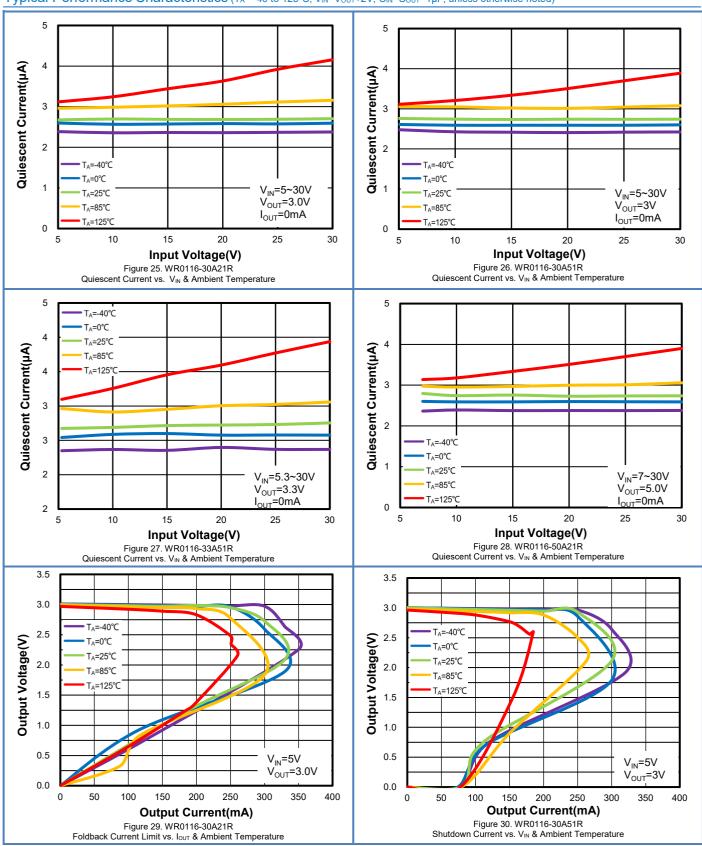
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100mA Ultra-low IQ, CMOS LDO

Typical Performance Characteristics (TA= -40 to 125°C, VIN=VOUT+2V, CIN=COUT=1µF, unless otherwise noted)

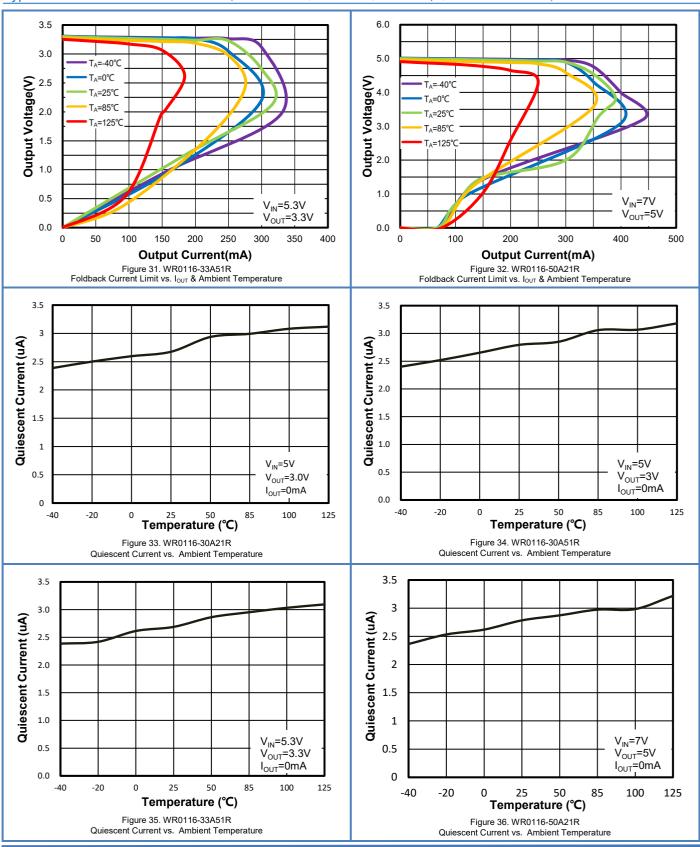


Typical Performance Characteristics (TA= -40 to 125°C, VIN=VOUT+2V, CIN=COUT=1µF, unless otherwise noted)



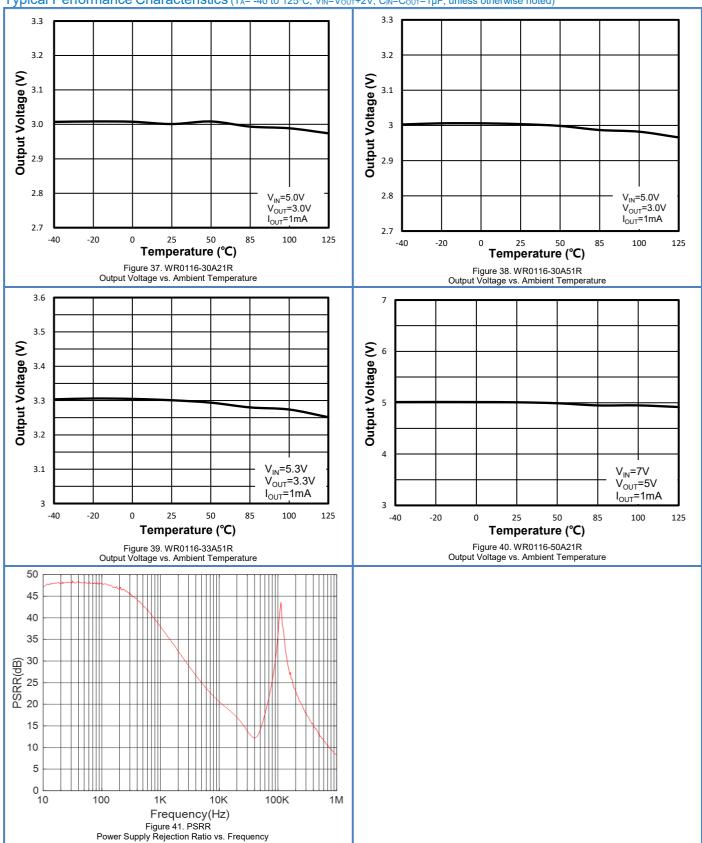


Typical Performance Characteristics (T_A= -40 to 125°C, V_{IN}=V_{OUT}+2V, C_{IN}=C_{OUT}=1µF, unless otherwise noted)



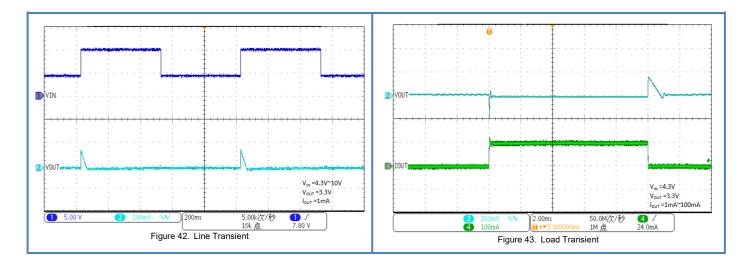
100mA Ultra-low IQ, CMOS LDO

Typical Performance Characteristics (T_A= -40 to 125°C, V_{IN}=V_{OUT}+2V, C_{IN}=C_{OUT}=1µF, unless otherwise noted)





Typical Performance Characteristics (TA= 25°C, VIN=VOUT+2V, CIN=COUT=1µF, unless otherwise noted)



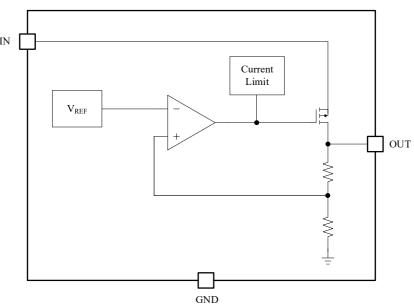
100mA Ultra-low IQ, CMOS LDO

11. Function Description

11.1 Overview

The WR0116 series is a set of low linear regulation, low load regulation, low power wide input voltage regulators implemented in CMOS technology, providing 100mA output current. The devices allow input voltages ranging from 3.5V to 30V, fixed version output voltages from 2.1V to 12V.

11.2 Block Diagram



11.3 Feature Description

11.3.1 Output Voltage Accuracy

The WR0116 has an output voltage accuracy of 3%. Output voltage accuracy is defined as the maximum and minimum error in output voltage. This includes the errors introduced by internal reference, load regulation and line regulation differences over the full range of rated load and line operating conditions, taking into account differences between manufacturing lots.

11.3.2 Dropout Voltage (V_{DO})

WR0116 is a low dropout voltage LDO that can achieve nominal output voltage at lower input voltages. Dropout voltage is defined as the V_{IN} - V_{OUT} at the rated maximum output current. When the input voltage is below the nominal output voltage, the output voltage varies with the input voltage. For CMOS regulators, the dropout voltage is determined by the R_{DS} (ON) of the pass-FET. The R_{DS} (ON) is calculated as follows:

11.3.3 Power Supply Rejection Ratio(PSRR)

PSRR, which stands for Power Supply Rejection Ratio, represents the ratio of the two voltage gains obtained when the input and output power supplies are considered as two independent sources. The basic calculation formula is

PSRR = 20log(Ripple(in) / Ripple(out))

100mA Ultra-low IQ, CMOS LDO

The units are in decibels (dB) and the logarithmic ratio is used.

The above equation shows that the output signal is influenced by the power supply in general, in addition to the circuit itself. PSRR is a quantity used to describe how the output signal is affected by the power supply; the larger the PSRR, the less the output signal is affected by the power supply.

As the level of integration continues to increase, the magnitude of supply current required is also increasing. End users want to extend battery life, i.e. they need very efficient DC/DC conversion processes, using more efficient switching regulators. However, switching regulators generate more—ripple in the power line than linear regulators.

The PSRR shows the ability of the LDO to suppress input voltage noise. For a clean, noise-free DC output voltage, use an LDO with a high PSRR.

Noise coupling from the input voltage to the internal reference voltage is the main cause of PSRR performance degradation. Using noise reduction capacitors at the input can effectively filter out noise and improve PSRR performance at low frequencies. The LDO can be used not only to regulate the voltage but also to provide an exceptionally clean DC supply for noise sensitive components.

The WR0116 is a high PSRR LDO that can be used not only for voltage regulation but also for noise cancellation in the power supply.

11.3.4 Foldback Current Limit (I_{CL})

In LDO circuits, if an output short circuit or excessive load current occurs, the device may be burned out. Especially in the case of a short circuit, not only is there too much current flowing through the regulator, but the voltage across the source drain of the regulator is also at its maximum, which is likely to burn out the regulator and make the device inoperable. The current limiting circuit used in LDO is a constant current limiting circuit, where the maximum load current that the LDO can supply is limited to a set constant I_{MAX} , and when an overload or short circuit occurs, the output current will be maintained at I_{MAX} , and the output voltage will be reduced to $I_{MAX}R_{LOAD}$.

However, if the external overload or short circuit condition lasts for a long time, the continuous high current will increase the device temperature and increase the power consumption of the whole system. To improve this situation, a foldback current limiting circuit can be used. In a foldback current limiting circuit, both the output current and the output voltage are gradually reduced when the output current reaches the set maximum current I_{MAX} . The output current is reduced to the set current threshold I_{FB} and the output voltage is reduced to $I_{FB}R_{LOAD}$. The output current is clamped to a smaller value in the event of an overload or short circuit and the system power consumption is reduced and the device temperature does not rise significantly.

The foldback current limiting circuit is essentially a constant current limiting circuit with an output voltage feedback loop, so that in the event of an overload or short circuit, the output current is gradually reduced due to the reduction in output voltage and eventually clamped at a smaller value.

100mA Ultra-low Iq. CMOS LDO

The WR0116 uses a foldback current limiting mode where the final current is clamped to around 70mA, thus providing good protection to the device.

More information on current limiting can be found in Electrical Characteristics *Figure 29* to *Figure 32*.

12. Application

Note: The information in the Applications section below is not part of WAY-ON's product specifications and WAY-ON does not guarantee its accuracy or completeness. The customer is responsible for determining the suitability of the component for its intended use and should verify and test its design implementation to confirm system functionality.

12.1 Application Information

The WR0116 is a linear voltage regulator with an input voltage of 3.5 V to 30 V and an output voltage of 2.1 V to 12 V. The accuracy is $\pm 3\%$. The maximum output current is 100 mA. The efficiency of a linear voltage regulator is determined by the ratio of the output voltage to the input voltage, so in order to achieve high efficiency, the differential voltage (V_{IN} - V_{OUT}) must be as small as possible. This section discusses how best to use this device in practical applications.

12.1.1 Start-Up

12.1.1.1. Automatic Discharge

The WR0116 has an internal pull-down MOSFET that connects a discharge resistor from V_{OUT} to ground to actively release the output voltage when the device is disabled.

12.1.2 Capacitor Recommendation

The WR0116 uses ceramic capacitors with low equivalent series resistance (ESR) at the V_{IN} and V_{OUT} pins to increase its stability. Multilayer ceramic capacitors are recommended. These capacitors also have limitations, and ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials have relatively good capacitance stability at different temperatures. WR0116 is designed to use ceramic capacitors of 1 μ F or larger at the input and output. Place C_{IN} and C_{OUT} as close to the IN and OUT pins as possible to minimize trace inductance from the capacitor to the device.

Increasing the input capacitance can reduce the transient input drop during start-up and load current. If the C_{OUT} produces high Q peak effects during transients, using only very large ceramic input capacitors can cause unwanted ringing at the OUT side, which requires well-designed short interconnects to the upstream supply to reduce ringing. Using a tantalum capacitor with an ESR of several hundred milliohms in parallel with the ceramic input capacitor can avoid unwanted ringing. The load step transient response is the output voltage response of the LDO to a step change in load current. A larger output capacitor reduces any voltage dips or spikes that occur during the load step, but at the same time the control loop bandwidth is reduced, which slows the response time.

Because, the LDO cannot consume charge, the control loop must close through the FET when the output load is removed or greatly reduced and wait for any excess charge to be depleted.

12.1.3 Power Dissipation(PD)

100mA Ultra-low IQ, CMOS LDO

The reliability of the circuit requires reasonable consideration of the power dissipation of the device, the location of the circuit on the PCB, and the proper sizing of the thermal plane. The regulator should be surrounded by no other heat generating devices as much as possible. The power dissipation of the regulator depends on the input and output voltage difference and the load conditions.

PD can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Using the proper input voltage minimizes the power dissipation, resulting in greater efficiency. To obtain the lowest power dissipation, use the minimum input voltage required for normal output voltage.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) of the device. Power dissipation and junction temperature are typically related to the junction-ambient thermal resistance (θ_{JA}) and ambient air temperature (T_A) of the PCB and package and are calculated as follows:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

The thermal resistance (θ_{JA}) depends primarily on the thermal dispersion capability of the PCB design. The total copper area, copper weight, and the location of the plane all affect the thermal dispersion capability, and the PCB and copper laydown area can only be used as a relative measure of the package's thermal performance.

12.1.4 Estimate the temperature of the junction

As recommended by JEDEC, the psi (Ψ) thermal metrics are used to estimate the junction temperature of the LDO in PCB board applications. These metrics are relative estimates of the junction temperature in actual applications. The thermal indicators Ψ_{JT} or Ψ_{JB} are given in the thermal information table and can be used according to the following equation.

$$\Psi_{JT}$$
: $T_J = T_T + \Psi_{JT} \times P_D$

$$\Psi_{JB}$$
: $T_J = T_B + \Psi_{JB} \times P_D$

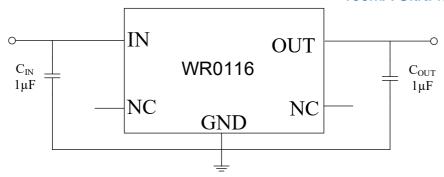
Notes.

- P_D is the power dissipated.
- T_T is the temperature at the top center of the device package.
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package.

12.2 Typical Application

This section discusses the application of the WR0116 in the circuit. The following figure shows the schematic of the application circuit.

Circuit schematic:



 C_{IN} and C_{OUT} are to be selected with the recommended appropriate capacitance. $1\mu F$ ceramic capacitors are selected for both C_{IN} and C_{OUT} to help balance the charge needed to charge the output capacitor during startup, thus reducing the input voltage drop.

13. Power supply recommendation

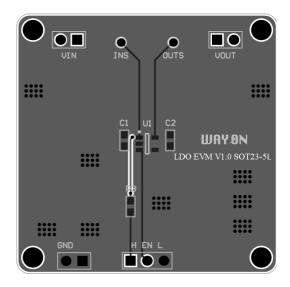
The WR0116 has a $V_{\rm IN}$ range of between 3.5V and 30V and an input capacitance of 1 μ F. The input voltage should have some redundancy to ensure a stable output voltage when the load fluctuates. If the input supply is noisy, additional input capacitors can be used to improve the noise performance of the output.

14. Layout Guidelines

The principle of LDO design is to place all components on the same side of the board and connect them as close as possible to their respective LDO pins. Connect the C_{IN} and C_{OUT} grounds, with all LDO ground pins as close together as possible, through a wide copper surface. Using through-holes and long wires for connections is strongly discouraged and can seriously affect system performance.

To improve thermal performance, an array of thermal vias is used to connect the thermal pad to the ground plane. A larger ground plane improves the thermal performance of the device and reduces the operating temperature of the device.

Layout Example:





15. Evaluation Modules

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

Name	Package	Evaluation Module
	SOT23-3L	WAYON LDO EVM V1.0 -SOT23-3L
WR0116	SOT23-5L	WAYON LDO EVM V1.0 - SOT23-5L
	SOT89-3L	WAYON LDO EVM V1.0 – SOT89-3L

16. Naming conventions

WR AA BB-CC DDD E

WR: WAYON Regulator

AA: 01/03/05/06 - Output Current, 100/300/500/600mA

BB: Serial number **CC:** Output Voltage

DDD: A31-Package, SOT23-3L A51-Package, SOT23-5L A21-Package, SOT89-3L

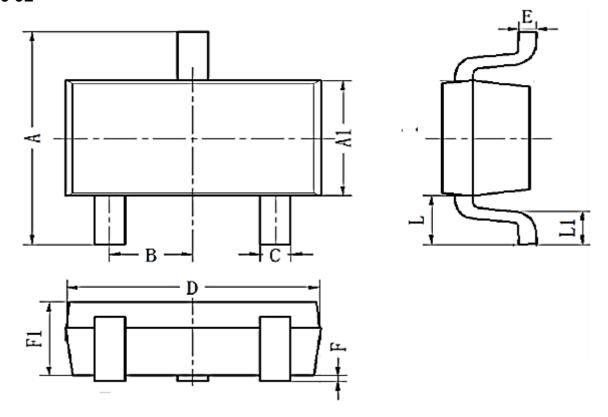
E: R-Reel & T-tube

17. Electrostatic discharge warning

ESD can cause irreversible damage to integrated circuits, ranging from minor performance degradation to device failure. Precision ICs are more susceptible to damage because very minor parameter changes can cause the device to be out of compliance with its published specifications. WAY-ON recommends that all ICs be handled with proper precautions. Failure to follow proper handling practices and installation procedures may damage the IC.

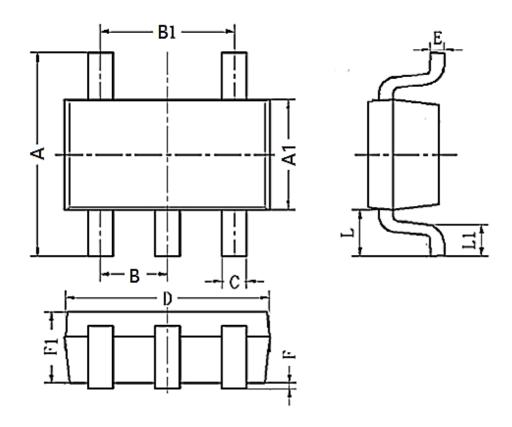
18. Package Information

SOT 23-3L



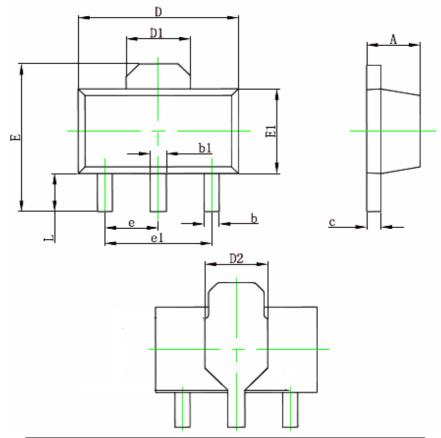
0)/44001	DIMENSIONS IN MILLIMETERS				
SYMBOL	MIN	NOM	MAX		
Α	2.60	2.80	3.00		
A 1	1.50	1.60	1.70		
В		0.95BSC			
С	0.25	0.40	0.50		
D	2.82	2.92	3.02		
E	0.10	0.15	0.20		
L		0.59REF			
L1	0.30	0.45	0.60		
F1	0.90	1.10	1.30		
F	0.00	0.08	0.15		

SOT 23-5L



0)/4501	DIMENSIONS IN MILLIMETERS				
SYMBOL	MIN	NOM	MAX		
Α	2.60	2.80	3.00		
A 1	1.50	1.60	1.70		
В		0.95BSC			
B1	1.90BSC				
С	0.25 0.40 0.50				
D	2.82	2.92	3.02		
Е	0.10	0.10 0.15 0.20			
F	0.00 0.08 0.15				
L	0.59REF				
F1	0.90	0.90 1.10 1.30			
L1	0.30	0.45	0.60		

SOT 89-3L



CVMDOL	DIMENS	IONS IN MILLIM	ETERS	
SYMBOL	MIN	NOM	MAX	
Α	1.4	1.5	1.6	
b	0.320	0.420	0.520	
b1	0.380	0.480	0.580	
С	0.350	0.405	0.460	
D	4.400	4.500	4.600	
D1	1.65REF			
D2	1.700 1.950 2		2.200	
Е	3.940	4.120	4.300	
E1	2.300	2.450	2.600	
е	1.5BSC			
e1	3.00BSC			
L	0.800 1.000 1.200			





19. Ordering Information

Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0116-21A31R	2.1V	SOT23-3L	3k/Reel	WR0116 21 XXXX
WR0116-22A31R	2.2V	SOT23-3L	3k/Reel	WR0116 22 XXXX
WR0116-25A31R	2.5V	SOT23-3L	3k/Reel	WR0116 25 XXXX
WR0116-27A31R	2.7V	SOT23-3L	3k/Reel	WR0116 27 XXXX
WR0116-28A31R	2.8V	SOT23-3L	3k/Reel	WR0116 28 XXXX
WR0116-30A31R	3.0V	SOT23-3L	3K/Reel	WR0116 30 XXXX
WR0116-33A31R	3.3V	SOT23-3L	3k/Reel	WR0116 33 XXXX
WR0116-36A31R	3.6V	SOT23-3L	3k/Reel	WR0116 36 XXXX
WR0116-44A31R	4.4V	SOT23-3L	3k/Reel	WR0116 44 XXXX
WR0116-45A31R	4.5V	SOT23-3L	3k/Reel	WR0116 45 XXXX
WR0116-50A31R	5.0V	SOT23-3L	3k/Reel	WR0116 50 XXXX
WR0116-A2A31R	12V	SOT23-3L	3k/Reel	WR0116 A2 XXXX
WR0116-21A51R	2.1V	SOT23-5L	3k/Reel	WR0116 21 XXXX
WR0116-22A51R	2.2V	SOT23-5L	3k/Reel	WR0116 22 XXXX
WR0116-25A51R	2.5V	SOT23-5L	3k/Reel	WR0116 25 XXXX
WR0116-27A51R	2.7V	SOT23-5L	3k/Reel	WR0116 27 XXXX
WR0116-28A51R	2.8V	SOT23-5L	3k/Reel	WR0116 28 XXXX
WR0116-30A51R	3.0V	SOT23-5L	3k/Reel	WR0116 30 XXXX
WR0116-33A51R	3.3V	SOT23-5L	3k/Reel	WR0116 33 XXXX
WR0116-36A51R	3.6V	SOT23-5L	3k/Reel	WR0116 36 XXXX
WR0116-44A51R	4.4V	SOT23-5L	3k/Reel	WR0116 44 XXXX
WR0116-45A51R	4.5V	SOT23-5L	3k/Reel	WR0116 45 XXXX
WR0116-50A51R	5.0V	SOT23-5L	3k/Reel	WR0116 50 XXXX
WR0116-A2A51R	12V	SOT23-5L	3k/Reel	WR0116 A2 XXXX
WR0116-21A21R	2.1V	SOT89-3L	1k/Reel	WR0116 21 XXXX
WR0116-22A21R	2.2V	SOT89-3L	1k/Reel	WR0116 22 XXXX
WR0116-25A21R	2.5V	SOT89-3L	1k/Reel	WR0116 25 XXXX
WR0116-27A21R	2.7V	SOT89-3L	1k/Reel	WR0116 27 XXXX
WR0116-28A21R	2.8V	SOT89-3L	1k/Reel	WR0116 28 XXXX
WR0116-30A21R	3.0V	SOT89-3L	1k/Reel	WR0116 30 XXXX
WR0116-33A21R	3.3V	SOT89-3L	1k/Reel	WR0116 33 XXXX



Part Number	Output Voltage	Package	Packing Quantity	Marking*
WR0116-36A21R	3.6V	SOT89-3L	1k/Reel	WR0116 36 XXXX
WR0116-44A21R	4.4V	SOT89-3L	1k/Reel	WR0116 44 XXXX
WR0116-45A21R	4.5V	SOT89-3L	1k/Reel	WR0116 45 XXXX
WR0116-50A21R	5.0V	SOT89-3L	1k/Reel	WR0116 50 XXXX
WR0116-A2A21R	12V	SOT89-3L	1k/Reel	WR0116 A2 XXXX

^{*} XXXX is variable.



STATEMENTS

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

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