WM02DN560Q

Dual N-Channel Enhancement Mode MOSFET

Description

WM02DN560Q uses advanced power trench technology that has been especially tailored to minimize the on-state resistance This device is suitable for un-directional or bidirectional load switch, facilitated by its common-drain configuration

$V_{(BR)DSS}$(V)	I_D(A)	$R_{DS(on)}$TYP (mΩ)
20	56	4.2 @VGS=4.5V
		4.3 @VGS=3.9V
		4.7 @VGS=3.1V
		5.0 @VGS=2.5V

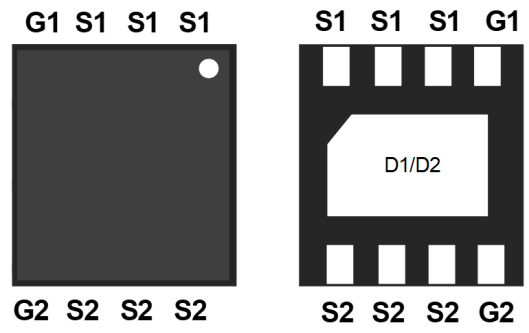
Features

- Super high dense cell for low $R_{DS(ON)}$
- RoHS Compliant and Halogen-Free
- ESD protected: Class 2

Applications

- Battery protection
- Load switch

Schematic & PIN Configuration



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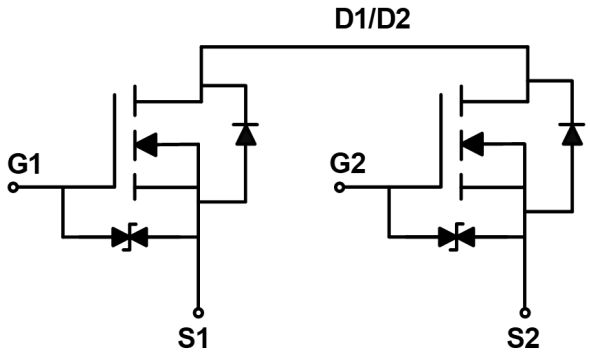


Device symbol

Absolute Maximum Rating (T_A= 25°C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_C=25°C	I_D	56	A
	T_C=100°C		35.6	
	T_A=25°C		20	
	T_A=70°C		15.8	
Pulsed Drain Current[1]		I_{DM}	100	A
Single Pulse Avalanche Energy[2]		EAS	64.8	mJ
Total Power Dissipation	T_C=25°C	P_D	31	W
	T_A=25°C		3.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	35	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	4	°C/W

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate-body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V	-	-	±10	μA
Gate-Threshold Voltage[3]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.45	-	1.0	V
Drain-Source on-Resistance[4]	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3A	3.5	4.2	5.4	mΩ
		V_{GS} = 3.9V, I_D = 3A	3.7	4.3	6	
		V_{GS} = 3.1V, I_D = 3A	3.8	4.7	6.2	
		V_{GS} = 2.5V, I_D = 3A	4	5	6.4	
Dynamic Characteristics[5]						
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} =0V, f =1MHz	-	3165	-	pF
Output Capacitance	C_{oss}		-	380	-	
Reverse Transfer Capacitance	C_{rss}		-	325	-	
Switching Characteristics[5]						
Total Gate Charge	Q_g	V_{GS} =3.9V, V_{DS} = 10V, I_D= 3A	-	33	-	
Gate-Source Charge	Q_{gs}		-	4.5	-	
Gate-Drain Charge	Q_{gd}		-	12	-	
Turn-on Delay Time	$t_{d(on)}$	V_{GS} =4.5V, V_{DD} = 16V, R_G = 6Ω, I_D= 3A	-	22	-	ns
Rise Time	t_r		-	41	-	
Turn-off Delay Time	$t_{d(off)}$		-	77	-	
Fall Time	t_f		-	21	-	
Drain-Source Diode Characteristics						
Diode Forward Voltage[4]	V_{SD}	I_S = 1A, V_{GS} = 0V	-	-	1.2	V

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=36A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

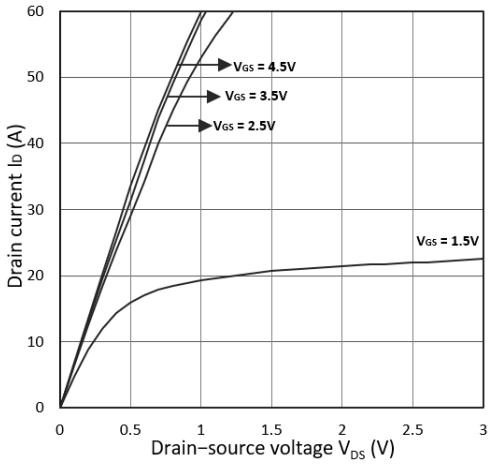


Figure 1. Output Characteristics

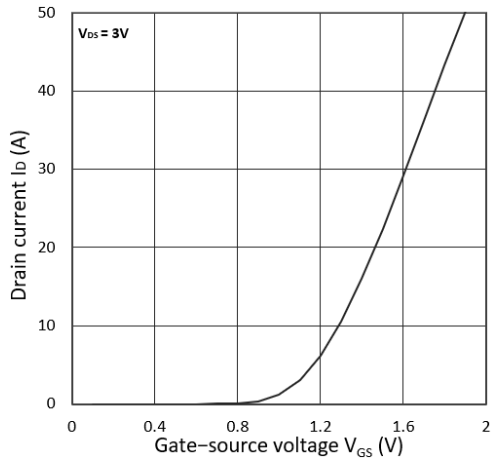


Figure 2. Transfer Characteristics

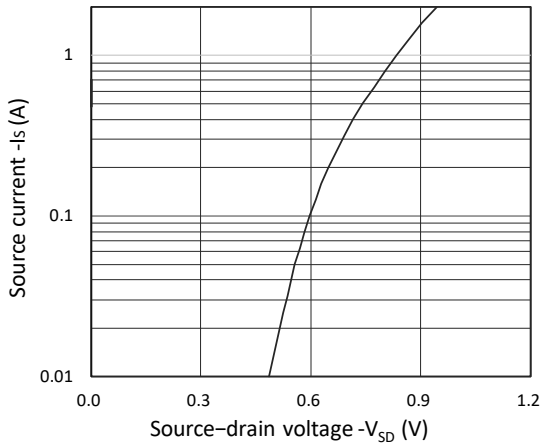


Figure 3. Forward Characteristics of Reverse

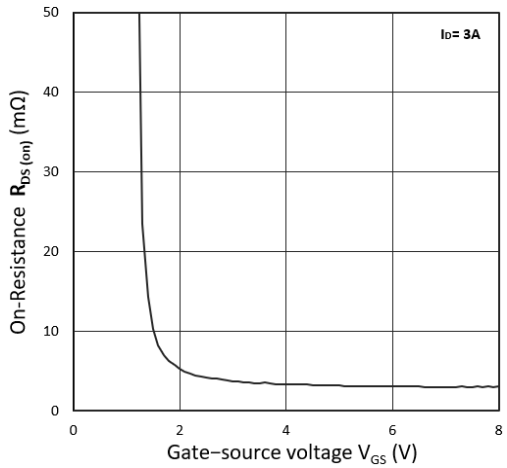


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

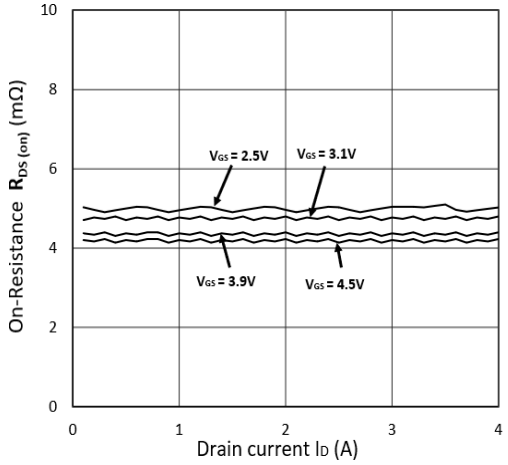


Figure 5. $R_{DS(ON)}$ vs. I_D

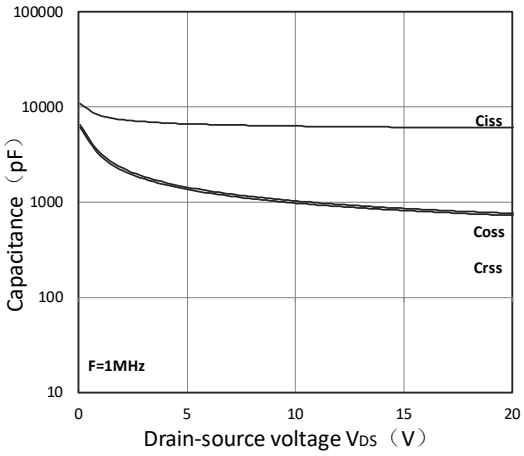
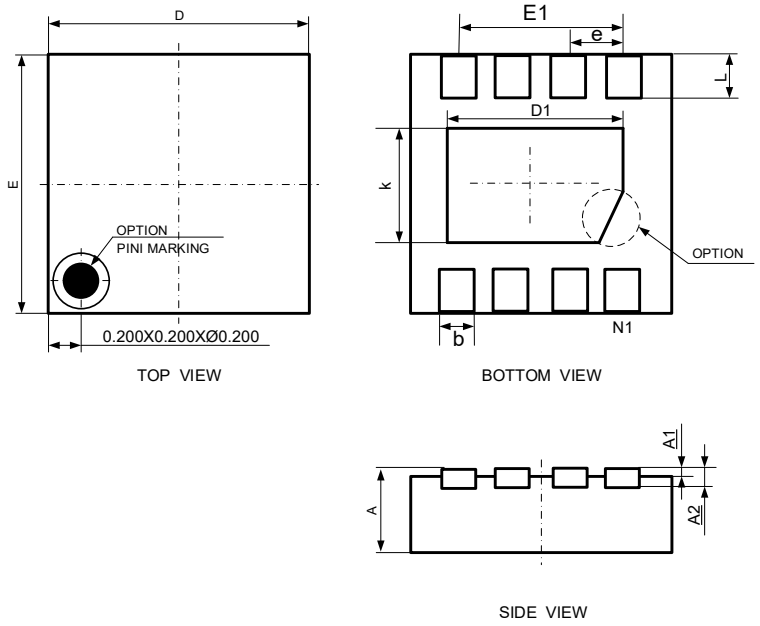
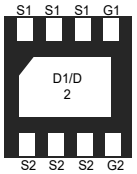


Figure 6. Capacitance Characteristics

Outline Drawing –DFN3030-8L

PACKAGE OUTLINE





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DIMENSIONS				
SYMBOL	MILLIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.027	0.031
A1	0.00	0.05	0.000	0.002
A2	0.203		0.008	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
E1	1.95REF		0.077BSC	
D1	2.20	2.40	0.087	0.094
K	1.40	1.60	0.055	0.063
b	0.25	0.35	0.009	0.014
e	0.65 BSC.		0.026BSC	
L	0.35	0.45	0.014	0.018

Marking Codes

Part Number	WM02DN560Q
Marking Code	Q56N02 WWXX XXX ● Q56N02 = Device code WWXX XXX= Date code

Package Information

Qty： 3k/Reel

CONTACT INFORMATION

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