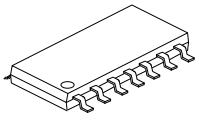
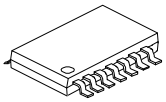
U74LVC07A

CMOS IC

HEX BUFFERS WITH OPEN-DRAIN OUTPUTS



SOP-14



TSSOP-14

■ DESCRIPTION

The **U74LVC07A** contain six independent buffers with open drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions

Inputs can be driven from 1.8V, 2.5V, 3.3V, or 5V devices. This feature allows the use of these devices as translators in a mixed-system environment.

■ FEATURES

* Operate from 1.65V to 5.5V
* Inputs and open-drain outputs accept voltages to 5.5V
* Direct interface with TTL levels
* I_{off} supports partial-power-down mode

■ ORDERING INFORMATION

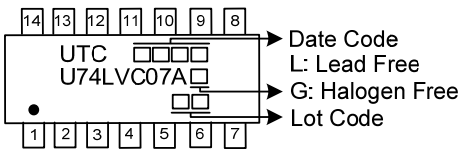
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC07AL-S14-R	U74LVC07AG-S14-R	SOP-14	Tape Reel
U74LVC07AL-P14-R	U74LVC07AG-P14-R	TSSOP-14	Tape Reel

U74LVC07AG-P14-R

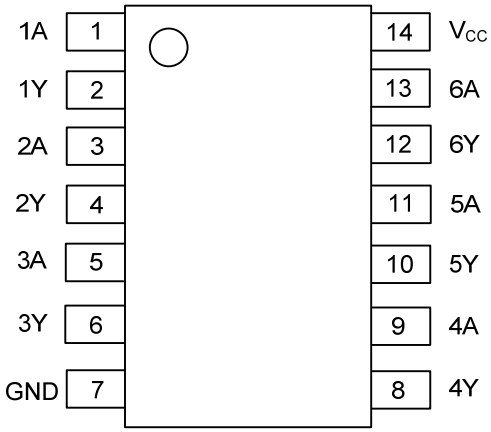
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

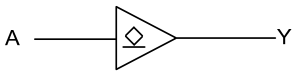


■ FUNCTION TABLE(each buffer)

INPUT(A)	OUTPUT(Y)
H	Z
L	L

Note: H: HIGH voltage level; L: LOW voltage level; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM(each inverter)



Logic symbol

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +6.5	V
Input Voltage	V_{IN}	-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
V_{CC} or GND Current	I_{CC}	±100	mA
Continuous Output Current (V_{OUT}=0 to V_{CC})	I_{OUT}	±50	mA
Input Clamp Current (V_{IN}<0)	I_{IK}	-50	mA
Output Clamp Current (V_{OUT}<0)	I_{OK}	-50	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Low-level Output Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			12	mA
		V_{CC}=2.7V			12	mA
		V_{CC}=3V			24	mA
		V_{CC}=4.5V			24	mA
Operating Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	113	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=1.65V ~ 1.95V	0.65×V_{CC}			V
		V_{CC}=2.3V ~ 2.7V	1.7			V
		V_{CC}=2.7V ~ 3.6V	2			V
		V_{CC}=4.5V ~ 5.5V	0.7×V_{CC}			V
Low-level Input Voltage	V_{IL}	V_{CC}=1.65V ~ 1.95V			0.35×V_{CC}	V
		V_{CC}=2.3V ~ 2.7V			0.7	V
		V_{CC}=2.7V ~ 3.6V			0.8	V
		V_{CC}=4.5V ~ 5.5V			0.3×V_{CC}	V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA			0.2	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=12mA			0.7	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3.0V, I_{OL}=24mA			0.55	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{IN}=5.5V or GND, V_{CC}=3.6V			±5	μA
Power OFF Leakage Current	I_{OFF}	V_{IN} or V_{OUT}=5.5V, V_{CC}=0V			±10	μA
Quiescent Supply Current	I_{CC}	V_{IN}= V_{CC} or GND, I_{OUT}=0 V_{CC}=3.6V			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=2.7 ~ 3.6V, I_{OUT}=0 One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_I	V_{IN}= V_{CC} or GND, V_{CC}=3.3V		5		pF

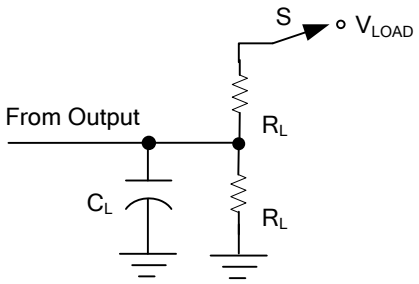
■ SWITCHING CHARACTERISTICS (T_A=-40~+125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (nA) to output(nY)	t_{PLZ} t_{PZL}	V_{CC}=1.8±0.15V,C_L=30pF, R_L=1KΩ	1		5.6	ns
		V_{CC}=2.5±0.2V,C_L=30pF, R_L=500Ω	1		3.4	ns
		V_{CC}=2.7V,C_L=50pF, R_L=500Ω			3.3	ns
		V_{CC}=3.3±0.3V,C_L=50pF, R_L=500Ω	1		3.6	ns
		V_{CC}=5±0.5V,C_L=50pF, R_L=500Ω	1		2.6	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

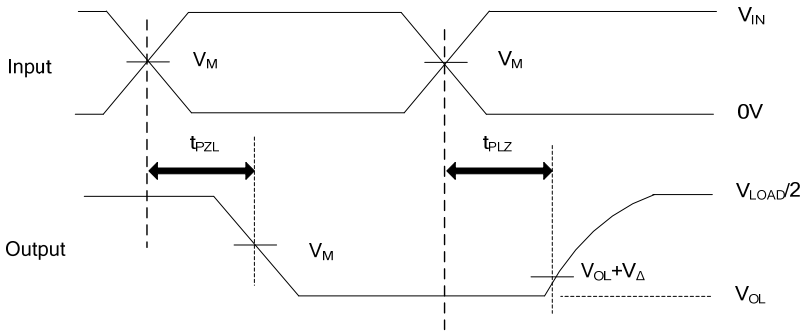
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per Inverter	C_{PD}	V_{CC}=1.8±0.15V, f=10MHz		1.8		pF
		V_{CC}=2.5±0.2V, f=10MHz		2.0		pF
		V_{CC}=3.3±0.3V, f=10MHz		2.5		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	V_{LOAD}	V_Δ	C_L	R_L
	V_{IN}	t_R, t_F					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	0.15V	30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	0.15V	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	2 x V_{CC}	0.3V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	2 x V_{CC}	0.3V	50pF	500Ω
5V±0.5V	Vcc	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	0.3V	50pF	500Ω



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.