# 8-Bit Shift Registers With 3-State Output

## 1 FEATURES

- **8-bit serial input, parallel output shift**
- **Serial Output (Q7S)**
- **Power-Supply Range: 2V to 5.5V**
- **Low power consumption: 160μA(Max)**
- **Low input current: 1μA(Max)**
- **Shift register has direct clear**
- **Storage register with 3-state outputs**
- **Extended Temperature: -40°C to +125°C**

## 2 APPLICATIONS

- **Enterprise and communications**
- **Industrial**
- **Personal electronics**
- **LED displays**
- **Servers**

## 3 DESCRIPTIONS

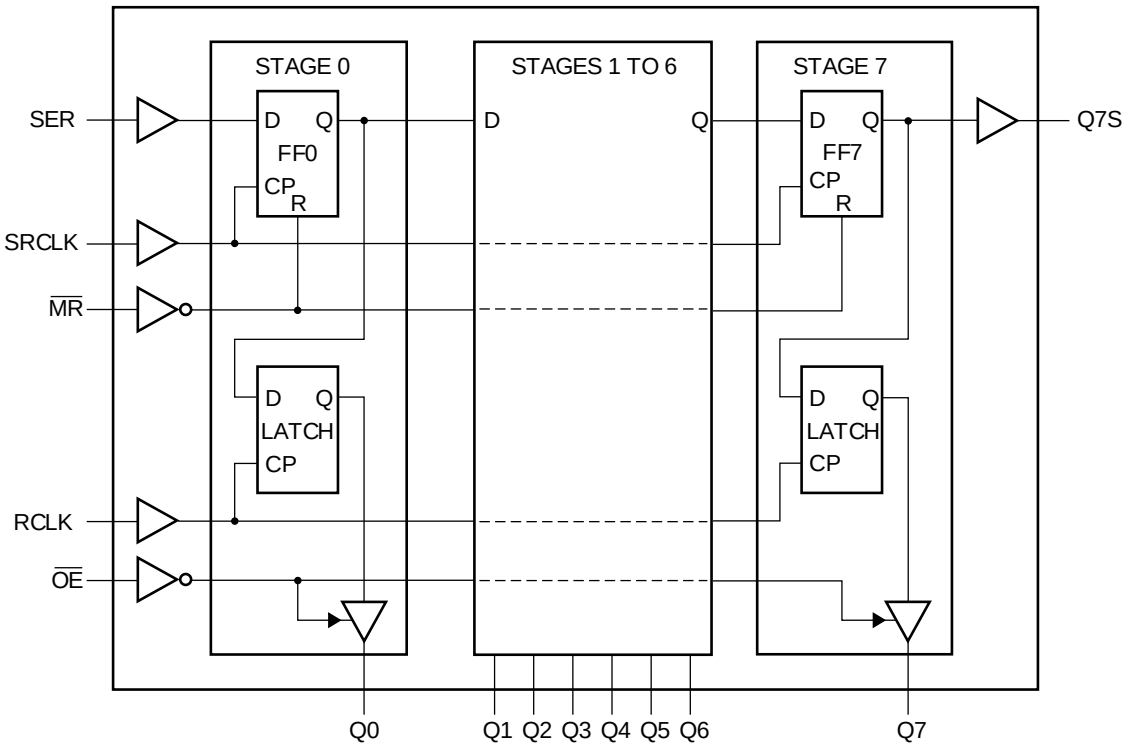
RS595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has an asynchronous reset ($\overline{MR}$) input, serial (SER) input, and serial outputs (Q7S) for cascading. A low on $\overline{MR}$ will clear the shift register. Data is shifted on the LOW-to-HIGH transitions of the SRCLK input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the RCLK input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is Low. A High on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers.

**Device Information (1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| RS595 | TSSOP-16 | 5.00mm×4.40mm |
| | SOIC-16(SOP16) | 9.90mm×3.90mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# 4 Functional Block Diagram



# Table of Contents

# 5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

| VERSION | Change Date | Change Item |
|---|---|---|
| A.1 | 2023/04/24 | Initial version completed |

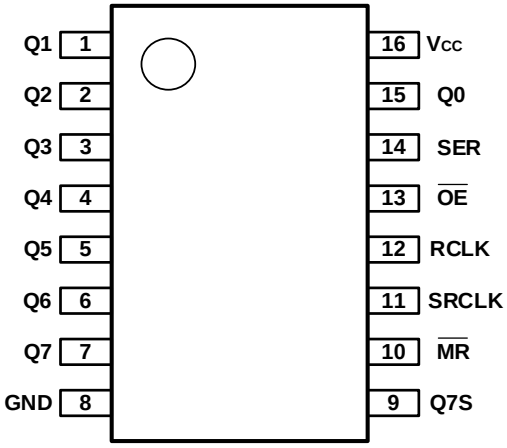
# 6 PACKAGE/ORDERING INFORMATION (1)

| PRODUCT | ORDERING NUMBER | TEMPERATURE RANGE | PACKAGE LEAD | PACKAGE MARKING (2) | MSL(3) | PACKAGE OPTION |
|---|---|---|---|---|---|---|
| RS595 | RS595XTSS16-G | -40°C ~+125°C | TSSOP-16 | RS595 | MSL1 | Tape and Reel,4000 |
| | RS595XS16-G | -40°C ~+125°C | SOIC-16(SOP16) | RS595 | MSL1 | Tape and Reel,4000 |

NOTE:
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

# 7 PIN CONFIGURATIONS

(TOP VIEW)




TSSOP-16/SOIC-16(SOP16)

## PIN DESCRIPTION

| PIN | NAME | TYPE (1) | FUNCTION |
|---|---|---|---|
| TSSOP-16/SOIC-16 | | | |
| 1~7 | Q1~Q7 | O | Parallel data output |
| 8 | GND | G | Ground. |
| 9 | Q7S | O | Serial data output |
| 10 | $\overline{MR}$ | I | Master reset (active Low) |
| 11 | SRCLK | I | Shift register clock input |
| 12 | RCLK | I | Storage register clock input |
| 13 | $\overline{OE}$ | I | Output enable input (active Low) |
| 14 | SER | I | Serial data input |
| 15 | Q0 | I | Parallel data output |
| 16 | $V_{CC}$ | P | Supply voltage |

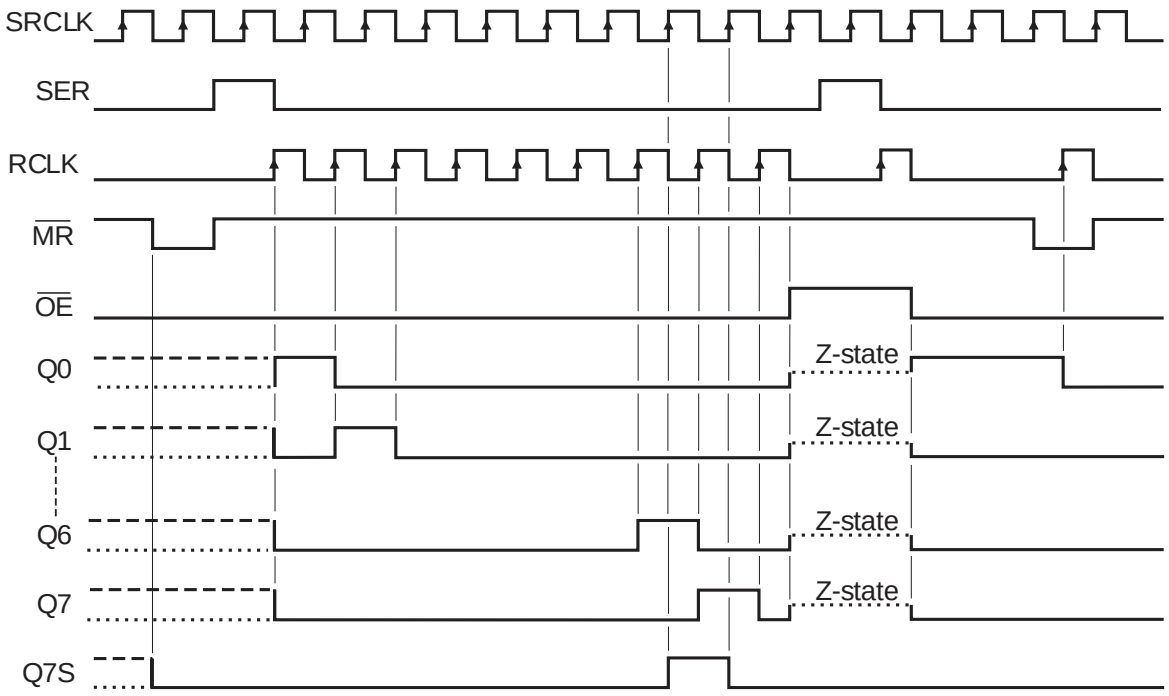
(1) I=input, O=output, P=power, G=Ground.

# 8 Functional description (1)

| CONTROL | | | | INPUT | OUTPUT | | FUNCTION |
|---|---|---|---|---|---|---|---|
| SRCLK | RCLK | $\overline{OE}$ | $\overline{MR}$ | SER | Q7S | Qn | |
| X | X | L | L | X | L | NC | a Low-level on $\overline{MR}$ only affects the shift registers |
| X | ↑ | L | L | X | L | L | empty shift register loaded into storage register |
| X | X | H | L | X | L | Z | shift register clear; parallel outputs in high-impedance OFF-state |
| ↑ | X | L | H | H | Q6S | NC | logic High-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S). |
| X | ↑ | L | H | X | NC | QnS | contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages |
| ↑ | ↑ | L | H | X | Q6S | QnS | contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages |

(1) H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW-to-HIGH transition;
X = don't care;
NC = no change;
Z = high-impedance OFF-state.

## 8.1 TIMING DIAGRAM



# 9 SPECIFICATIONS

## 9.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Range | | -0.5 | 6.5 | V |
| $I_{IK}$ | Input Clamp Current | $V_I$ < -0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_{OK}$ | Output Clamp Current | $V_O$ < -0.5V or $V_O$ > $V_{CC}$+0.5V | | ±20 | mA |
| $I_O$ | Output Current | $V_O$=-0.5V to ($V_{CC}$+0.5V) | | | |
| | | Pin Q7S | | ±25 | mA |
| | | Pin Qn | | ±35 | mA |
| $I_{CC}$ | Supply Current | | | 70 | mA |
| $I_{GND}$ | Ground Current | | -70 | | mA |
| $\theta_{JA}$ | Package thermal impedance (2) | TSSOP-16 | | 45 | °C/W |
| | | SOIC-16(SOP16) | | 150 | |
| $T_J$ | Junction Temperature (3) | | -40 | 150 | °C |
| $T_{stg}$ | Storage Temperature | | -65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |
| | | Machine Model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

**ESD SENSITIVITY CAUTION**

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.3 Recommended Operating Conditions

Voltages are reference to GND(0V).

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 2.0 | | 5.5 | V |
| High-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | 1.40 | | | V |
| | | $V_{CC}$=4.5V | 3.15 | | | |
| | | $V_{CC}$=5.5V | 3.85 | | | |
| Low-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | | 0.60 | V |
| | | $V_{CC}$=4.5V | | | 1.35 | |
| | | $V_{CC}$=5.5V | | | 1.65 | |
| Input voltage | $V_I$ | | 0 | | $V_{CC}$ | V |
| Output voltage | $V_O$ | | 0 | | $V_{CC}$ | V |
| Input transition rise or fall rate(Δt/Δv) | Data inputs | $V_{CC}$=2.0V | | | 625 | ns/V |
| | | $V_{CC}$=4.5V | | | 139 | |
| | | $V_{CC}$=5.5V | | | 83 | |
| Operating temperature | $T_A$ | | -40 | | 125 | °C |

## 9.4 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TEMP | MIN(1) | TYP(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | all outputs | | | | | | V |
| | | $I_O$ = -20 μA | 2.0 V | FULL | 1.9 | | | |
| | | | 4.5V | | 4.4 | | | |
| | | | 5.5V | | 5.4 | | | |
| | | Q7S output | | | | | | |
| | | $I_O$ = -4 mA | 4.5V | FULL | 3.8 | | | |
| | | $I_O$ = -5.2 mA | 5.5V | | 4.8 | | | |
| | | Qn bus driver outputs | | | | | | |
| | | $I_O$ = -6 mA | 4.5V | FULL | 3.7 | | | |
| | | $I_O$ = -7.8 mA | 5.5V | | 4.7 | | | |
| $V_{OL}$ | | all outputs | | | | | | V |
| | | $I_O$ = 20 μA | 2.0 V | FULL | | | 0.1 | |
| | | | 4.5V | | | | 0.1 | |
| | | | 5.5V | | | | 0.1 | |
| | | Q7S output | | | | | | |
| | | $I_O$ = 4 mA | 4.5V | FULL | | | 0.2 | |
| | | $I_O$ = 5.2 mA | 5.5V | | | | 0.3 | |
| | | Qn bus driver outputs | | | | | | |
| | | $I_O$ = 6 mA | 4.5V | FULL | | | 0.3 | |
| | | $I_O$ = 7.8 mA | 5.5V | | | | 0.35 | |
| $I_I$ | input leakage Current | $V_I$=$V_{CC}$ or GND | 5.5V | FULL | | | ±1 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I$=$V_{IH}$ or $V_{IL}$; $V_O$=$V_{CC}$ or GND | 5.5V | FULL | | | ±10 | |
| $I_{CC}$ | supply current | $V_I$=$V_{CC}$ or GND; $I_O$=0A | 5.5V | FULL | | | 160 | |
| $\Delta I_{CC}$ | additional supply current | per input pin; $I_O$ = 0A; $V_I$ = $V_{CC}$-0.6V; other inputs at $V_{CC}$ or GND; | 4.5V-5.5V | FULL | | | 100 | μA |
| $C_I$ | input capacitance | $V_I$=$V_{CC}$ or GND | 5.5V | FULL | | 6 | | pF |

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

## 9.5 Switching Characteristics

over recommended operating free-air temperature range, Full=-40°C to 125°C. (1)

| PARAMETER | -40°C to +125°C | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CC}$=2.0V (2) | | | $V_{CC}$=4.5V (2) | | | $V_{CC}$=5.5V (2) | | | |
| | MIN | TYP(3) | MAX | MIN | TYP(3) | MAX | MIN | TYP(3) | MAX | |
| Propagation delay,$t_{pd}$(4) SRCLK to Q7S | | | 51 | | | 20 | | | 18 | ns |
| Propagation delay, $t_{pd}$ RCLK to Qn | | | 53 | | | 23 | | | 21 | ns |
| High to Low propagation, $\overline{MR}$ to Q7S, $t_{PHL}$(5) | | | 40 | | | 18 | | | 16 | ns |
| Enable time,$t_{en}$(6) $\overline{OE}$ to Qn | | | 51 | | | 23 | | | 21 | ns |
| Disable time,$t_{dis}$(7) $\overline{OE}$ to Qn | | | 69 | | | 42 | | | 41 | ns |
| Pulse width,$t_w$ SRCLK High or Low | 110 | | | 22 | | | 19 | | | ns |
| Pulse width,$t_w$ RCLK High or Low | 110 | | | 22 | | | 19 | | | ns |
| Pulse width,$t_w$ $\overline{MR}$ Low | 110 | | | 22 | | | 19 | | | ns |
| Hold width,$t_h$ SER to SRCLK | 3 | | | 3 | | | 3 | | | ns |
| Set-up time,$t_{su}$ SER to SRCLK | 55 | | | 11 | | | 10 | | | ns |
| Set-up time,$t_{su}$ SRCLK to RCLK | 110 | | | 22 | | | 19 | | | ns |
| Recovery time $t_{rec}$ $\overline{MR}$ to SRCLK | 50 | | | 10 | | | 9 | | | ns |
| Maximum frequency $f_{max}$ SRCLK/RCLK $C_L$=15pF | 4 | | | 20 | | | 24 | | | MHz |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) Typical values are measured at nominal supply voltage.
(4) $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.
(5) $t_{pd}$ is the same as $t_{PHL}$ only.
(6) $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
(7) $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

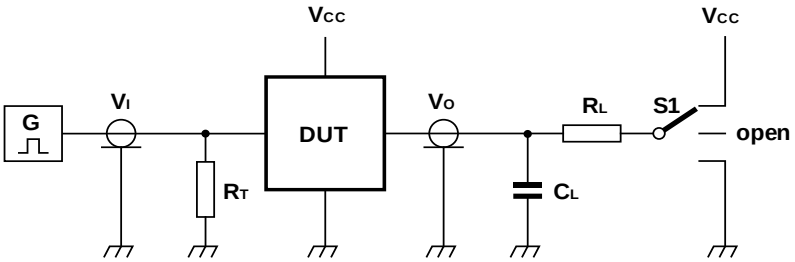
## 9.6 Operating Characteristics

$T_A$=25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$(1) | SER = 1 MHz; SRCL = RCLK = 10MHz; $V_I$ = GND to $V_{CC}$ (2)(3) | 115 | pF |

(1) Power dissipation capacitance per transceiver.
(2) $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_O)$ where:
$f_i$ = input frequency in MHz;
$f_O$ = output frequency in MHz;
$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V.
(3) All 9 outputs switching.

## 10 Parameter Measurement Information




LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PHL}/t_{PLH}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| $V_I$ | $V_{CC}$ |
| $t_r/t_f$ | 9ns |
| $C_L$ | 50pF |
| $R_L$ | 1KΩ |

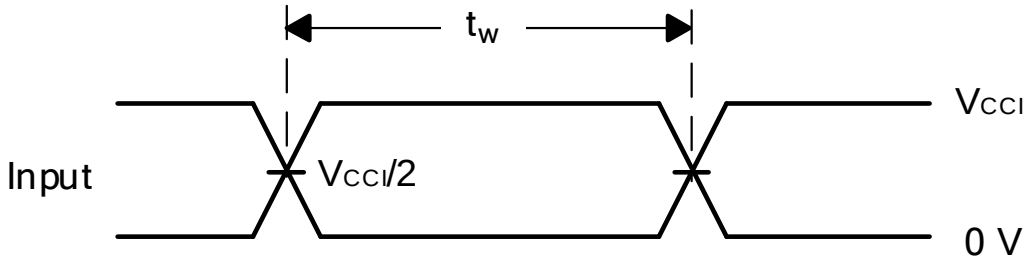



**Figure 1. Voltage Waveforms Pulse Duration**

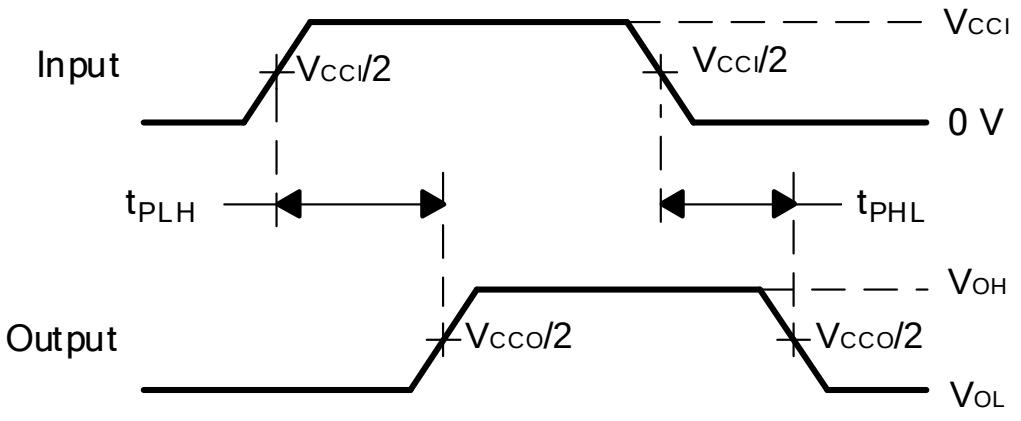



**Figure 2. Voltage Waveforms Propagation Delay Times**

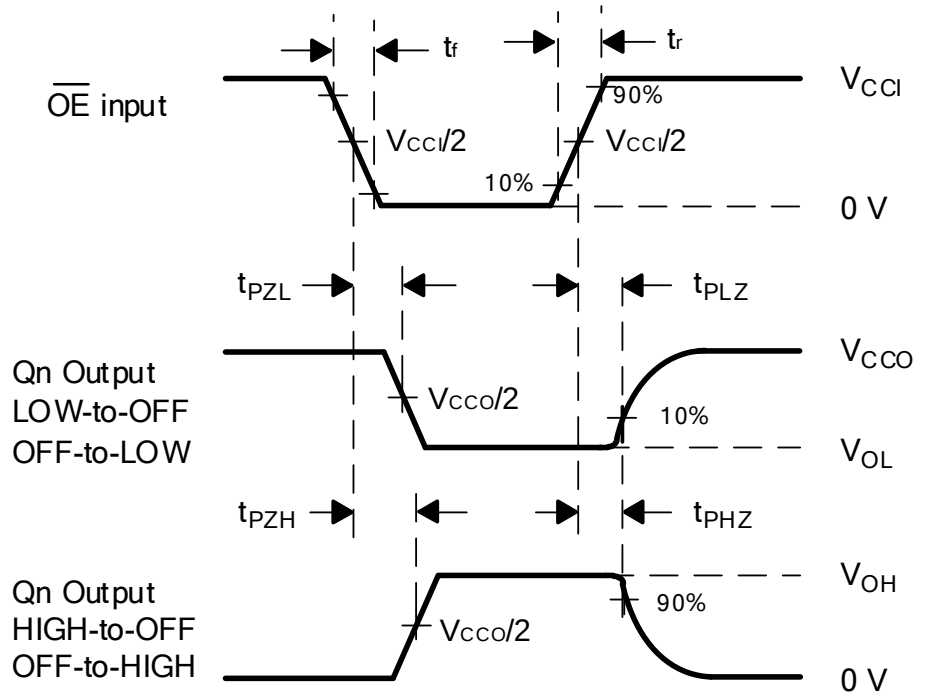



**Figure 3. Voltage Waveforms Enable and Disable Times**

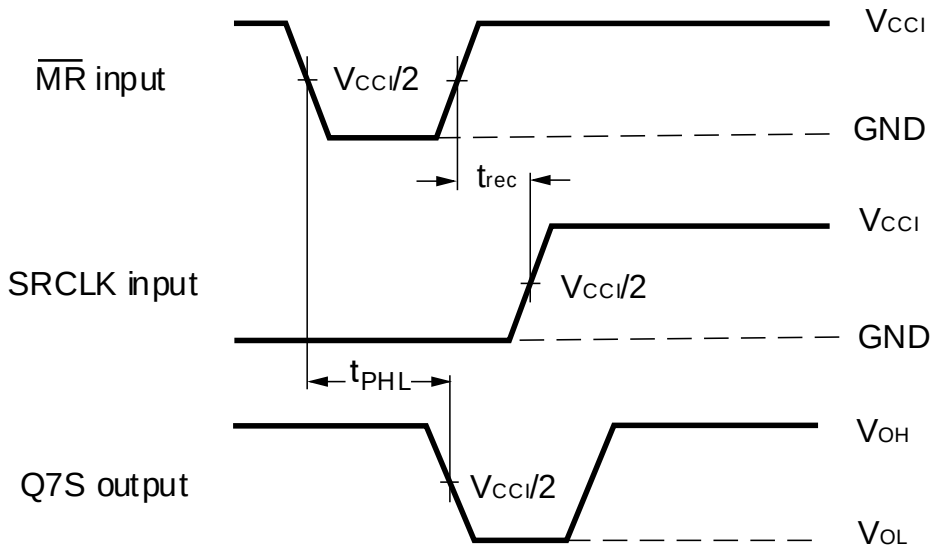



**Figure 4. Master Reset to Output Propagation Delays**

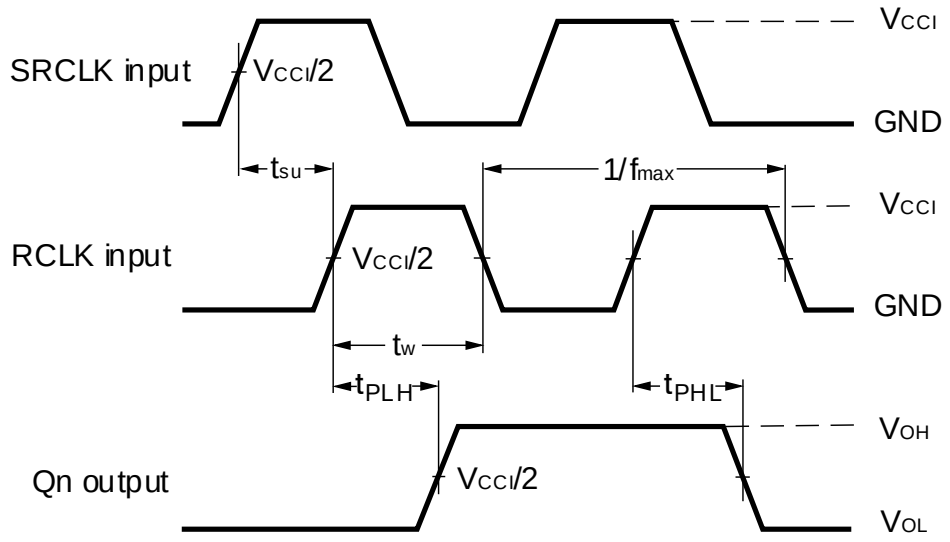



**Figure 5. Storage Clock to Output Propagation Delays**

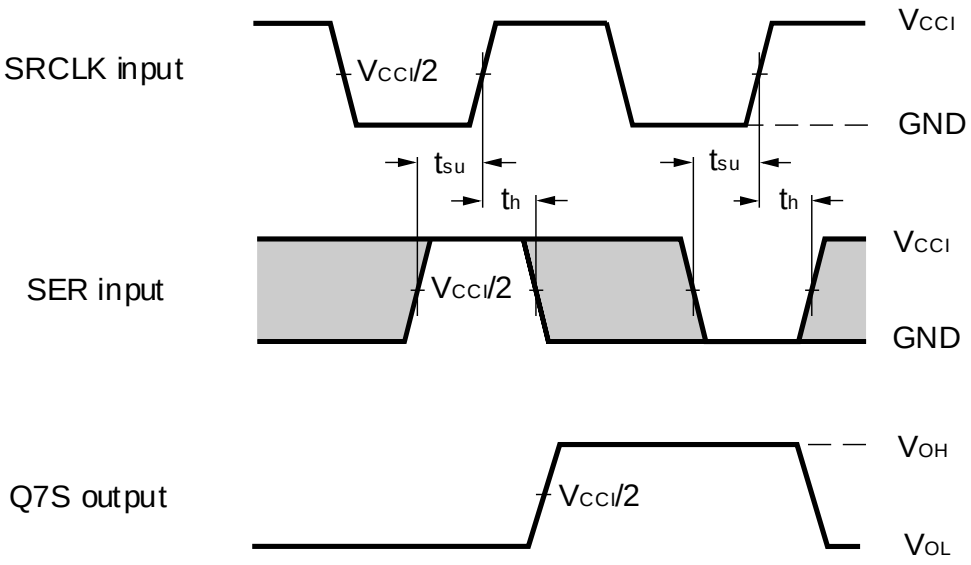
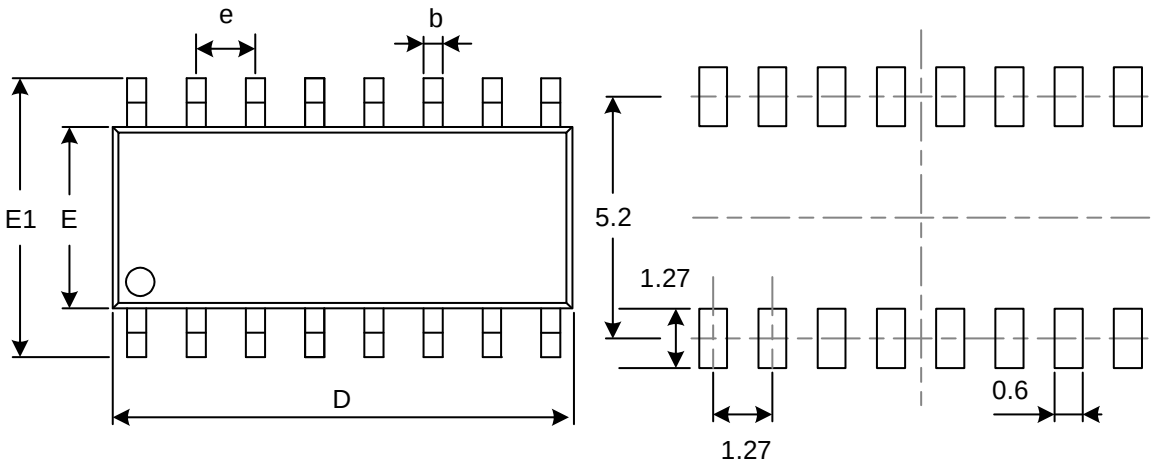



**Figure 6. Data Set-up and Hold Times**

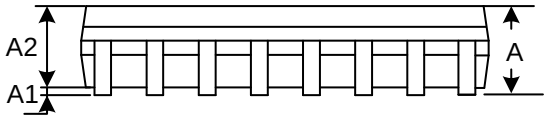
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, $Z_O$ = 50 Ω，dv/dt≥1V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
E. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. All parameters and waveforms are not applicable to all devices.
H. The shaded areas indicate when the input is permitted to change for predictable output performance.
I. $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

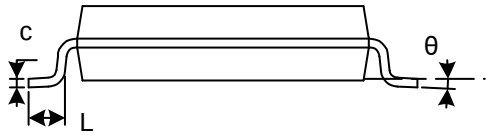
# 11 PACKAGE OUTLINE DIMENSIONS

## SOIC-16(SOP16)



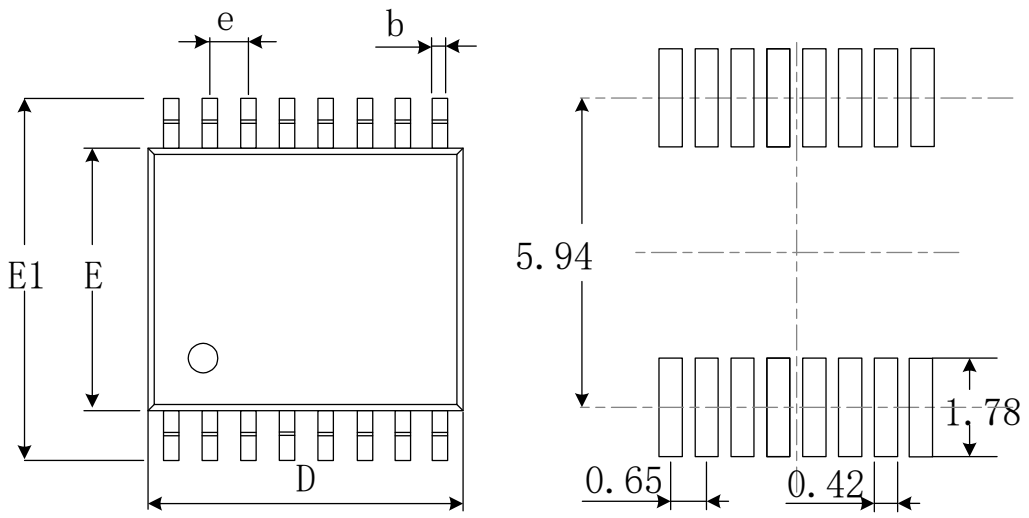

**RECOMMENDED LAND PATTERN** (Unit: mm)



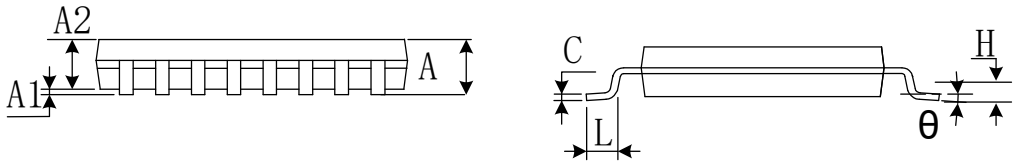




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 1.750 | | 0.069 |
| A1 | 0.100 | 0.225 | 0.004 | 0.009 |
| A2 | 1.300 | 1.500 | 0.051 | 0.059 |
| b | 0.390 | 0.470 | 0.015 | 0.019 |
| c | 0.200 | 0.240 | 0.007 | 0.010 |
| D | 9.800 | 10.00 | 0.386 | 0.394 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.500 | 0.800 | 0.020 | 0.032 |
| θ | 0° | 8° | 0° | 8° |

## TSSOP-16




**RECOMMENDED LAND PATTERN** (Unit: mm)

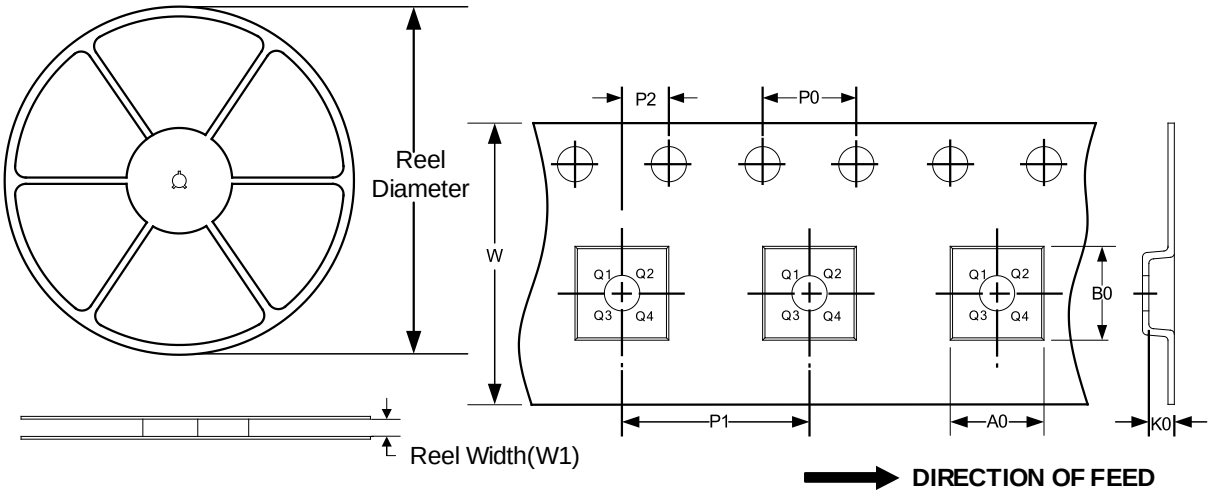



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 1.200 | | 0.047 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.900 | 1.050 | 0.035 | 0.041 |
| b | 0.200 | 0.280 | 0.007 | 0.011 |
| c | 0.130 | 0.170 | 0.005 | 0.007 |
| D | 4.900 | 5.100 | 0.193 | 0.201 |
| E | 4.300 | 4.500 | 0.169 | 0.177 |
| E1 | 6.200 | 6.600 | 0.244 | 0.260 |
| e | 0.650(BSC) | | 0.026(BSC) | |
| L | 0.450 | 0.750 | 0.017 | 0.030 |
| H | 0.250 TYP | | 0.010 TYP | |
| θ | 0° | 8° | 0° | 8° |

# 12 TAPE AND REEL INFORMATION

## REEL DIMENSIONS

## TAPE DIMENSION




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width(mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOIC-16(SOP16) | 13'' | 16.4 | 6.50 | 10.30 | 2.10 | 4.0 | 8.0 | 2.0 | 16.0 | Q1 |
| TSSOP16 | 13'' | 12.4 | 6.90 | 5.60 | 1.20 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

# IMPORTANT NOTICE AND DISCLAIMER

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