Low Power Configurable Multiple-Function Gate

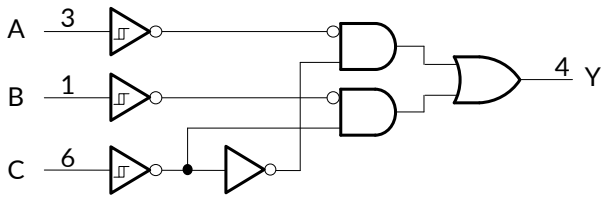
1 FEATURES

- **Operating Voltage Range:1.65V to 5.5V**
- **Low Power Consumption:10μA (Max)**
- **Operating Temperature Range: -40°C to +125°C**
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at V_{CC}=3.0V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection**
- **Micro SIZE PACKAGES: SOT23-6, SOT363(SC70-6)**

2 APPLICATIONS

- **Cable Solutions**
- **Barcode Scanners**
- **E-Books**
- **Embedded PC**
- **Network-Attached Storage**
- **Video Communications Systems**
- **Servers**
- **Wireless Data Access Cards, Headsets, Keyboard, Mouse, and LAN Cards**

Logic Diagram (Positive Logic)



3 DESCRIPTIONS

The RS1G97 configurable multiple-function gate is designed for 1.65V to 5.5V V_{CC} operation.

The RS1G97 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

The RS1G97 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

This device available in Green SOT23-6 and SOT363(SC70-6) packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1G97	SOT23-6(6)	1.60mm×2.92mm
	SOT363 (SC70-6)(6)	2.10mm×1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	L	L	L
L	H	L	H
H	H	L	H
L	L	H	L
H	L	H	H
L	H	H	L
H	H	H	H

H=High Voltage Level
L=Low Voltage Level

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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/01/10	Initial version completed
A.2	2023/09/01	Add MSL on Page 4@RevA.1

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1G97	RS1G97XH6	-40°C ~+125°C	SOT23-6	1G97	MSL3	Tape and Reel,3000
	RS1G97XC6	-40°C ~+125°C	SC70-6 (SOT363)	1G97	MSL3	Tape and Reel,3000

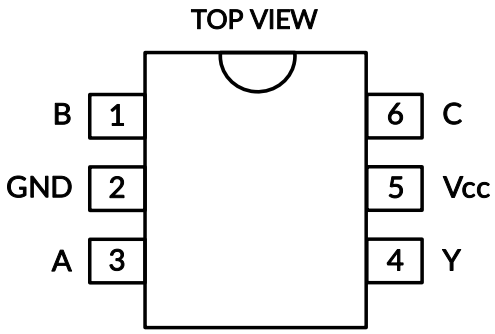
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS



SOT23-6/SOT363(SC70-6)

PIN DESCRIPTION

PIN	NAME	I/O TYPE (1)	FUNCTION
SOT23-6/SOT363(SC70-6)			
1	B	I	Data Input
2	GND	P	Ground
3	A	I	Data Input
4	Y	O	Data output
5	V_{CC}	P	Supply Power
6	C	I	Data Input

(1) I=input, O=output, P=power.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	SOT23-6		230	°C/W
		SOT363(SC70-6)		265	
T_J	Junction temperature (5)		-65	150	°C
Tstg	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions table*.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

9.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
Operating temperature	T_A		-40	+125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

9.2 DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{T+}	Positive going input threshold voltage		1.65V	Full	0.75		1.05	V
			2.3V		1.25		1.55	
			3V		1.5		2.1	
			4.5V		2.3		3.0	
			5.5V		2.8		3.4	
V_{T-}	Negative going input threshold voltage		1.65V	Full	0.3		0.6	V
			2.3V		0.35		0.65	
			3V		0.45		0.75	
			4.5V		0.7		1.0	
			5.5V		0.85		1.15	
ΔV_T	Hysteresis (V_{T+}-V_{T-})		1.65V	Full	0.35		0.6	V
			2.3V		0.6		1.2	
			3V		1.05		1.65	
			4.5V		1.6		2.0	
			5.5V		1.95		2.25	
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	Input	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI_{CC}		One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i (Input Capacitance)		V_I=V_{CC} or GND	3.3V	+25°C		4		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

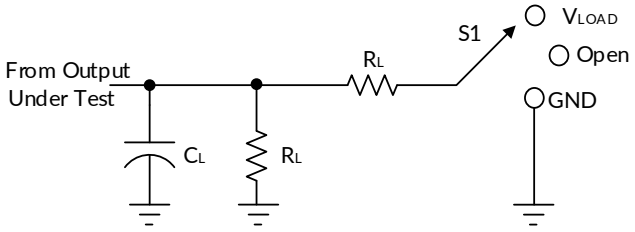
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

9.3 AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
Propagation Delay	t_{pd}	V_{CC}=1.8V±0.15V	C_L=30pF, R_L=500Ω		7.8		ns
		V_{CC}=2.5V±0.2V	C_L=30pF, R_L=500Ω		3.5		
		V_{CC}=3.3V±0.3V	C_L=50pF, R_L=500Ω		3.1		
		V_{CC}=5V±0.5V	C_L=50pF, R_L=500Ω		2.6		
Power dissipation capacitance	C_{pd}	V_{CC}=1.8V	f=10MHz		20		pF
		V_{CC}=2.5V			21		
		V_{CC}=3.3V			22		
		V_{CC}=5V			25		

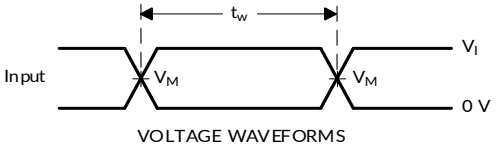
(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

10 Parameter Measurement Information

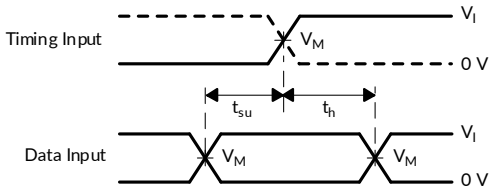


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

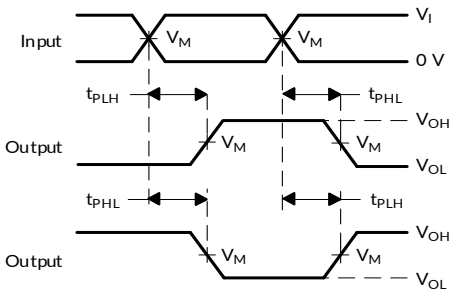
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L		R_L		V_Δ
	V_I	t_r/t_f							
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	15pF	50pF	1MΩ	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	15pF	50pF	1MΩ	500Ω	0.3V



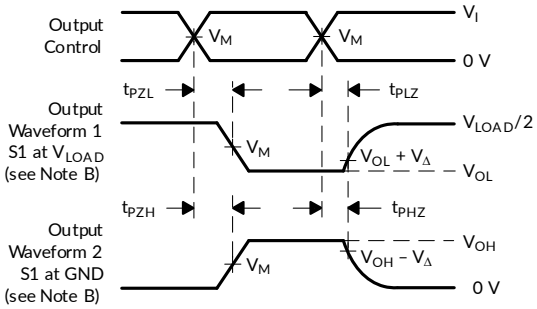
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

11 Detailed Description

11.1 Overview

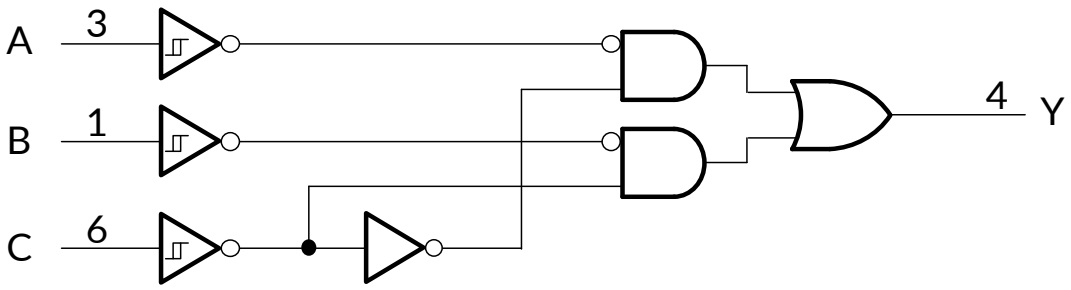
This configurable multiple-function gate is designed for 1.65V to 5.5V V_{CC} operation.

The RS1G97 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose variations of common logic functions, like MUX, AND, OR, and NOT. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

This device is fully-specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

11.2 Functional Block Diagram



11.3 Feature Description

The RS1G97 device has a wide operating V_{CC} range of 1.65 V to 5.5 V, which allows use in a broad range of systems. The 5.5V I/Os allow down translation and also allow voltages at the inputs when V_{CC} = 0 V.

11.4 Device Functional Modes

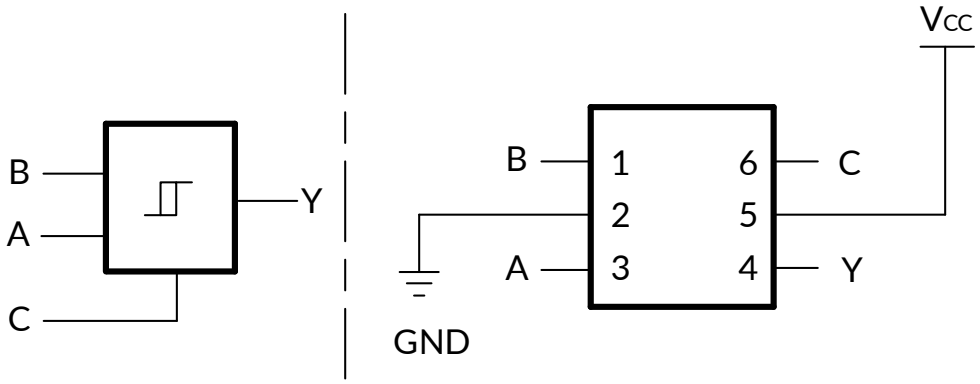


Figure 2. Two-Input MUX

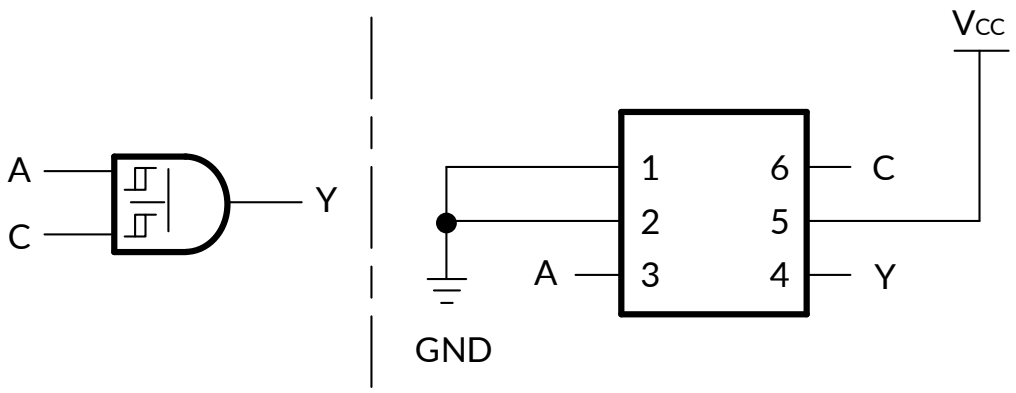


Figure 3. Two-Input AND Gate

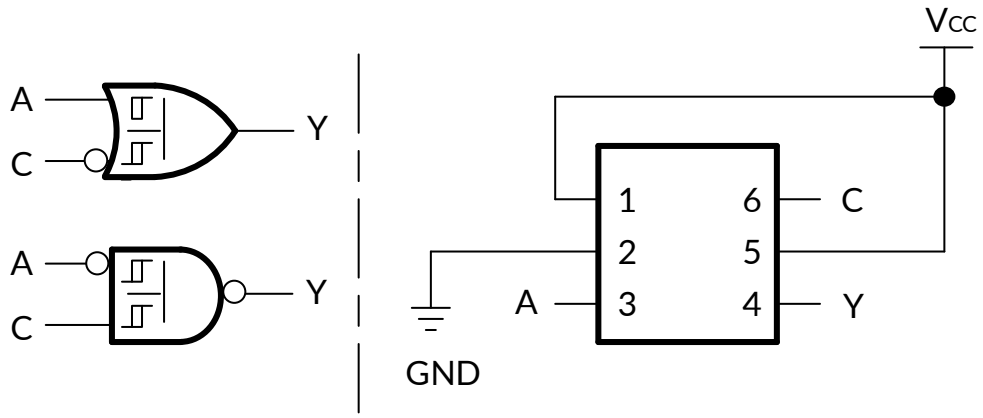


Figure 4. Two-Input OR with one input inverted or Two-Input NAND with one input inverted

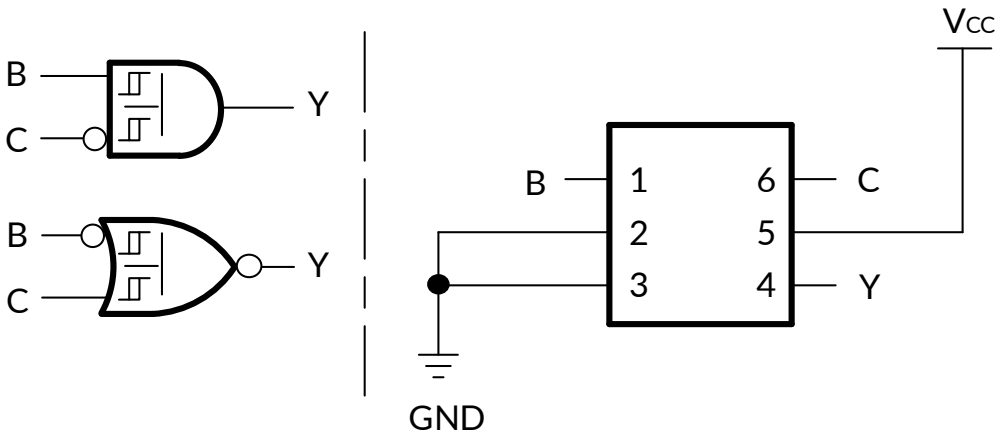


Figure 5. Two-Input AND with one input inverted or Two-Input NOR with one input inverted

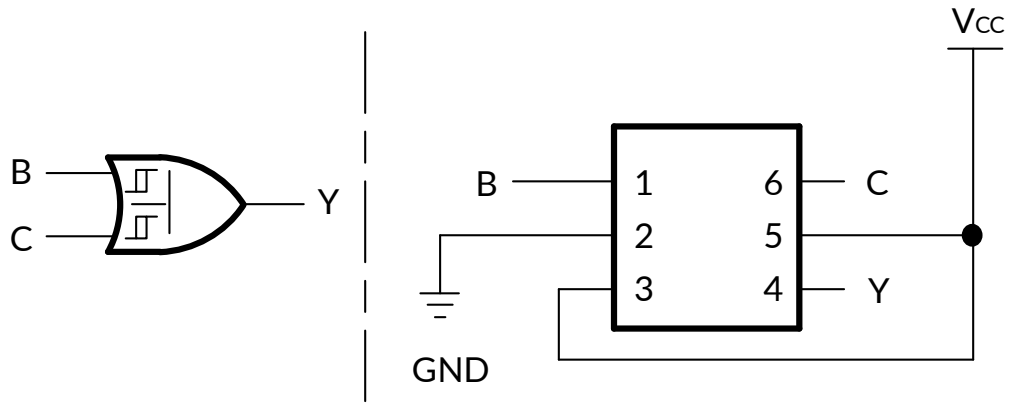


Figure 6. Two-Input OR Gate

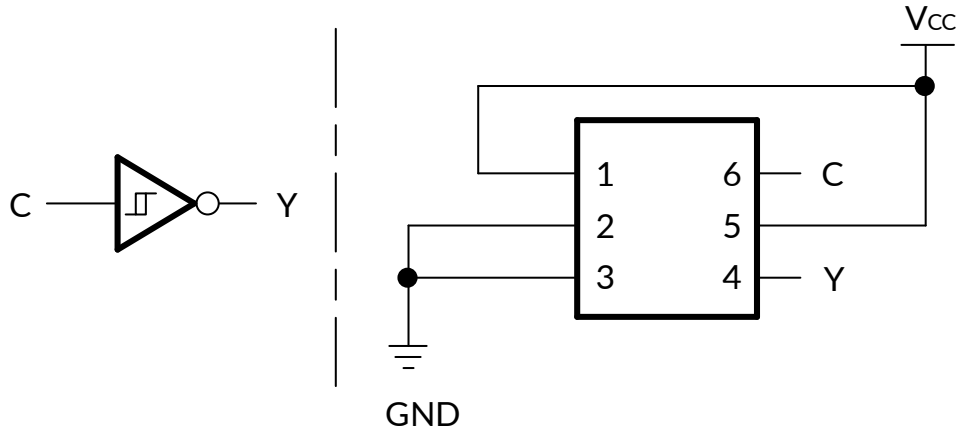


Figure 7. Inverter

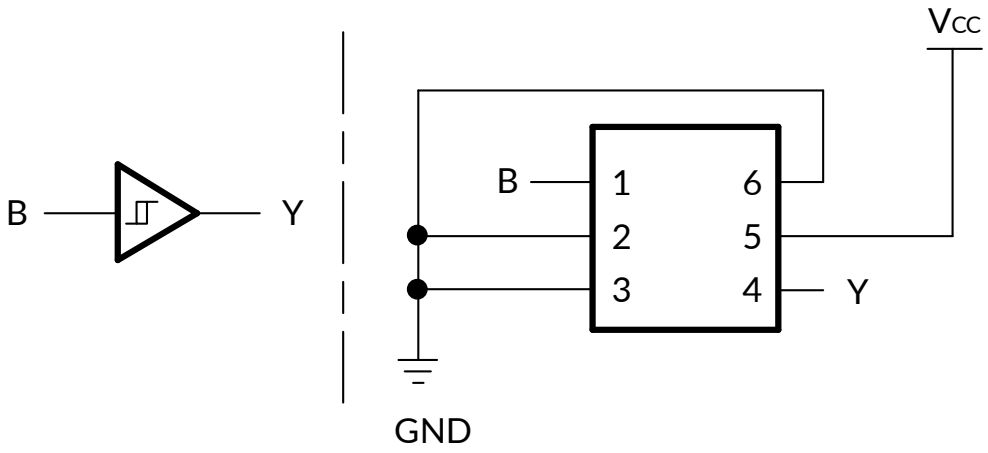


Figure 8. Buffer

12 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

The RS1G97 device offers flexible configuration for many design applications. This example describes basic power sequencing using the AND gate configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning.

12.2 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

The RS1G97 allows for performing logical Boolean functions with digital signals. Maintain input signals as close as possible to either 0 V or V_{CC} for optimal operation.

13 Power Supply Recommendations

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1uF capacitor is recommended and if there are multiple V_{CC} terminals then 0.01uF or 0.022uF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

14 Layout

14.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/O_S so they also cannot float when disabled.

14.2 Layout Example

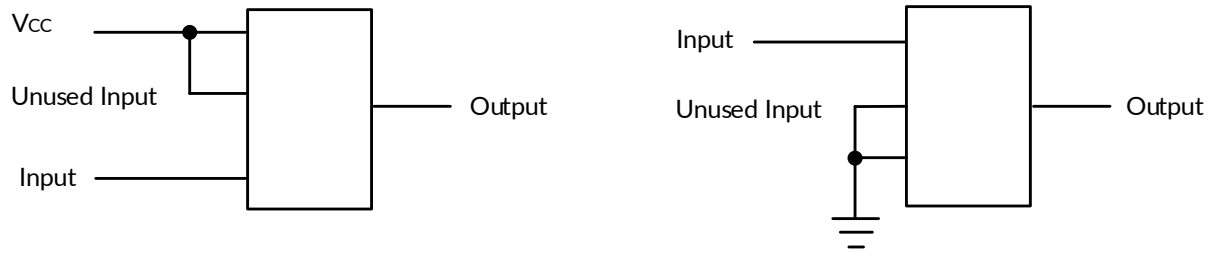
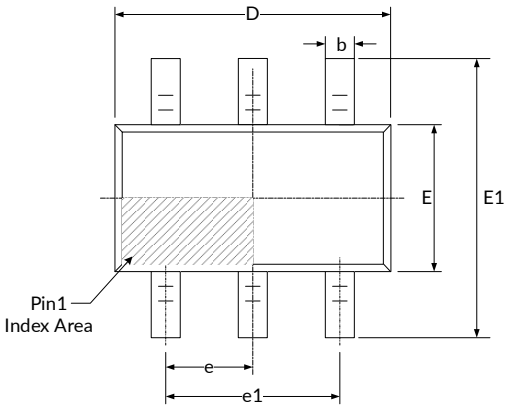
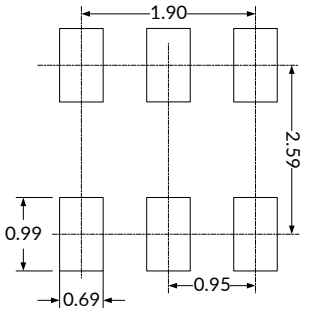


Figure 9. Layout Diagram

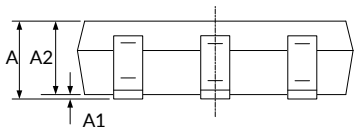
15 PACKAGE OUTLINE DIMENSIONS

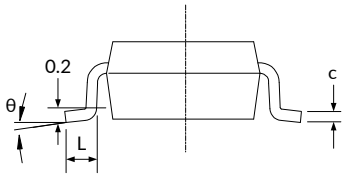
SOT23-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



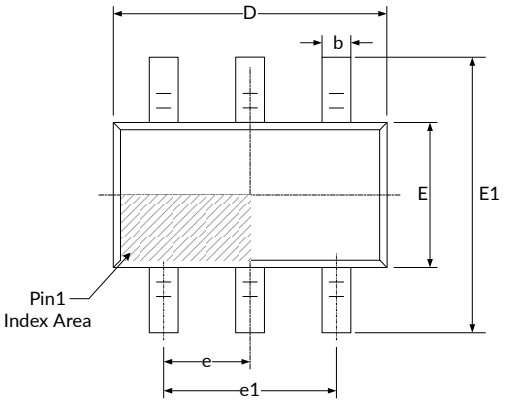


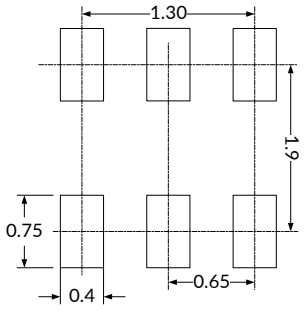
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

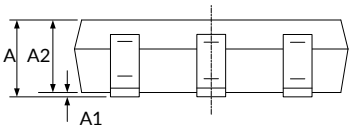
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

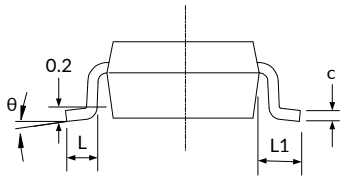
SOT363(SC70-6) [3]





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A [1]	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D [1]	2.000	2.200	0.079	0.087
E [1]	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) [2]		0.026(BSC) [2]	
e1	1.300(BSC) [2]		0.051(BSC) [2]	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

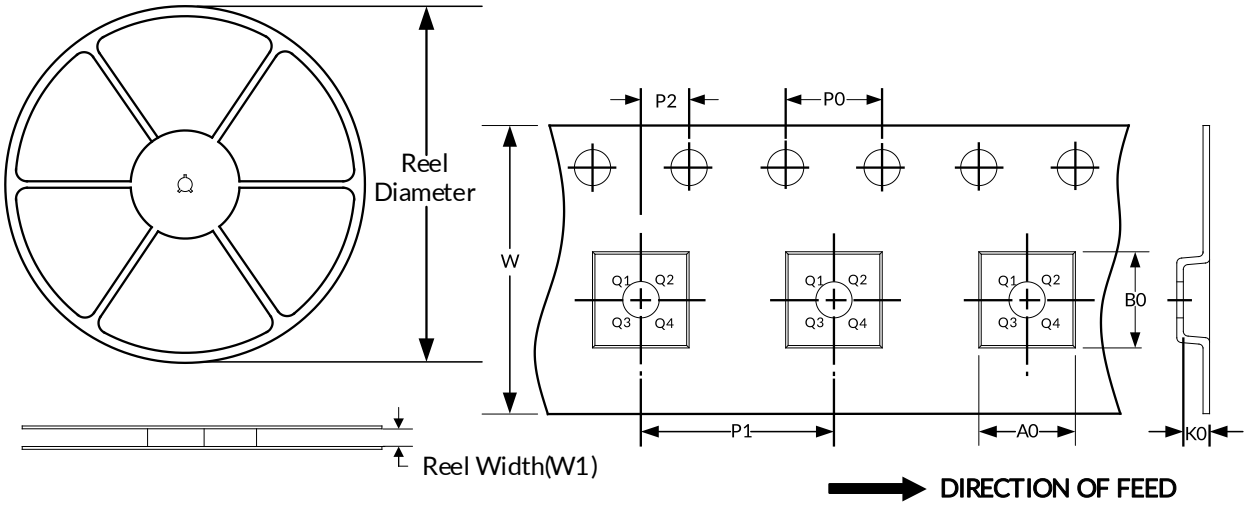
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

16 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT363(SC70-6)	7”	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT23-6	7”	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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