

Description

JMT P-channel Enhancement Mode Power MosFET

Features

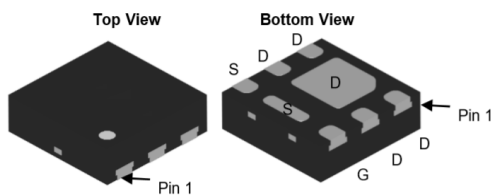
- -20V, -15A
 $R_{DS(ON)} < 15.1m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 20.7m\Omega @ V_{GS} = -2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

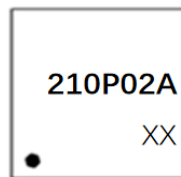
- Load Switch
- PWM Application
- Power Management



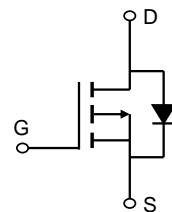
100% UIS TESTED!
100% ΔVds TESTED!



DFN2020-6L



Marking and Pin



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
210P02A	JMTV210P02A	TAPING	DFN2020-6L	7"	3000	120000

Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-15
		$T_A = 100^\circ\text{C}$	-9.5
I_{DM}	Pulsed Drain Current ⁽¹⁾	-60	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	25	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.6
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	49	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	-	-	-1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.8	-1.0	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -4.5V, I _D = -10A	-	11.6	15.1	mΩ
		V _{GS} = -2.5V, I _D = -5A	-	15.9	20.7	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz	-	1797	-	pF
C _{oss}	Output Capacitance		-	213	-	pF
C _{rss}	Reverse Transfer Capacitance		-	180	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -4.5V V _{DS} = -10V, I _D = -10A	-	16	-	nC
Q _{gs}	Gate Source Charge		-	4	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	3	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{GS} = -4.5V, V _{DD} = -10V I _D = -10A, R _{GEN} = 3Ω	-	8	-	ns
t _r	Turn-On Rise Time		-	35	-	ns
t _{d(off)}	Turn-Off Delay Time		-	71	-	ns
t _f	Turn-Off Fall Time		-	70	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-15	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-60	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -15A	-	-	-1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = -10A, di/dt = 100A/us	-	10	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	3	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. EAS condition: Starting T_J=25C, V_{DD}=-15V, V_G=-10V, R_G=25ohm, L=0.5mH, I_{AS}=-10A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

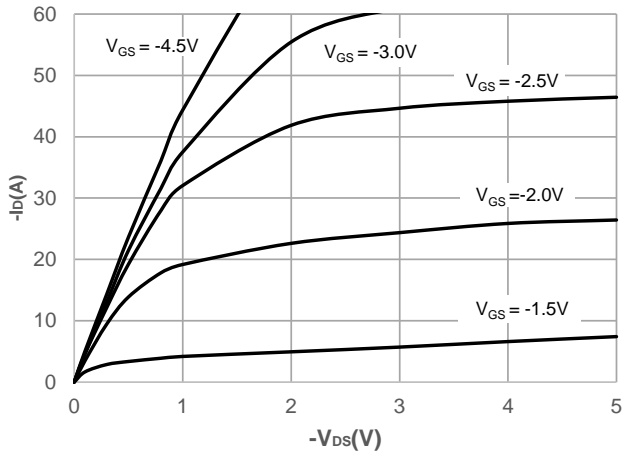


Figure 2: Typical Transfer Characteristics

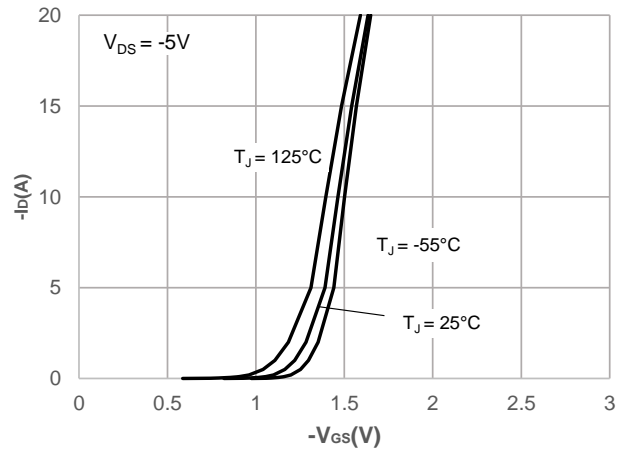


Figure 3: On-resistance vs. Drain Current

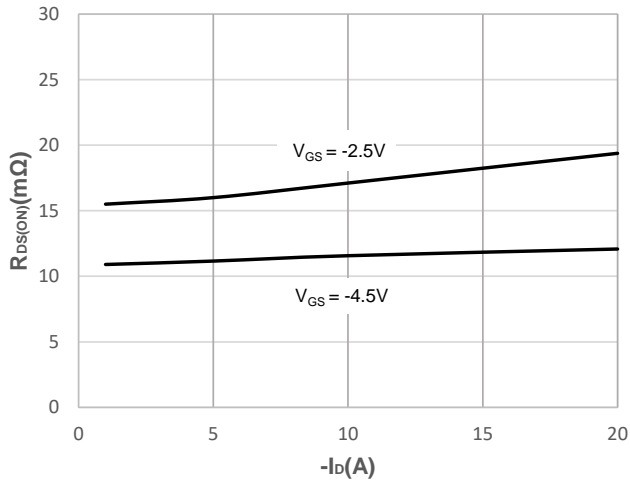


Figure 4: Body Diode Characteristics

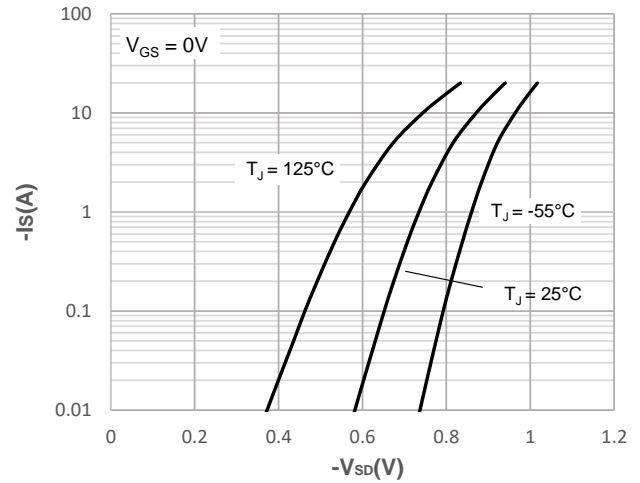


Figure 5: Gate Charge Characteristics

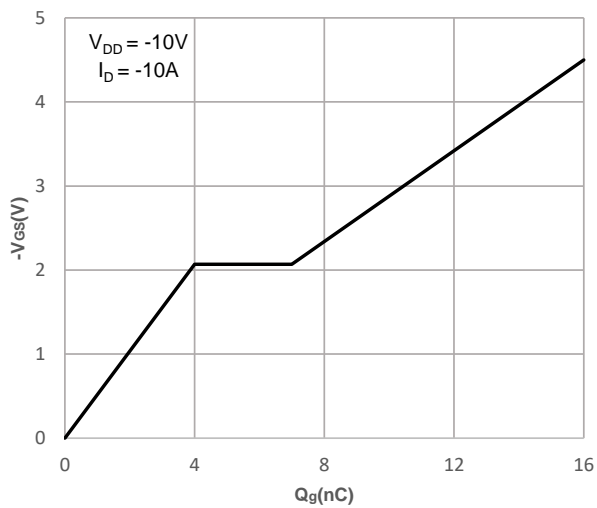
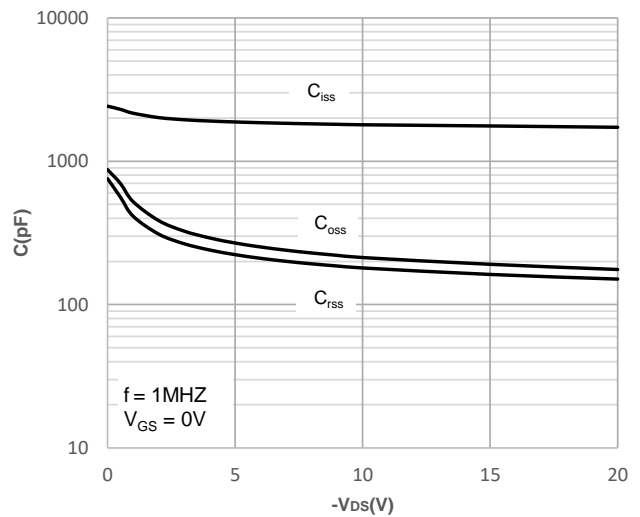


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

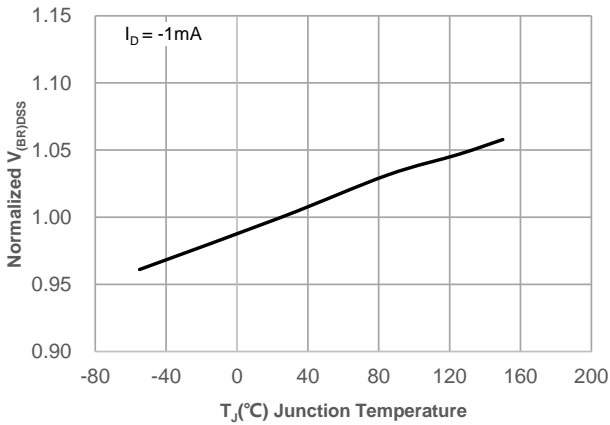


Figure 8: Normalized on Resistance vs. Junction Temperature

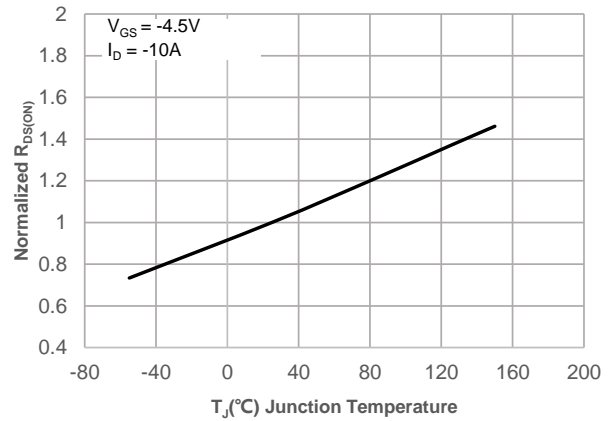


Figure 9: Maximum Safe Operating Area

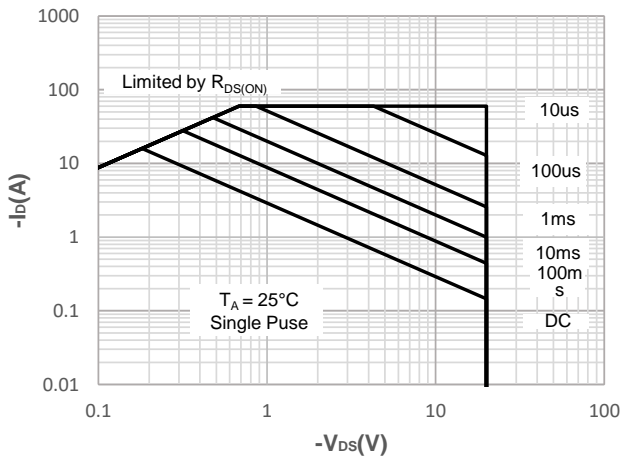


Figure 10: Maximum Continuous Driand Current vs. Ambient Temperature

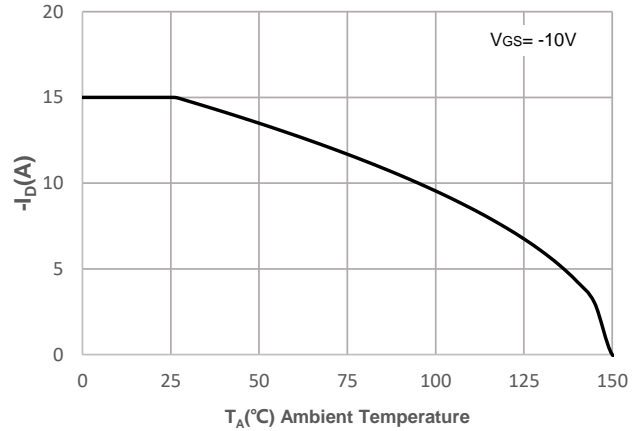


Figure 11: Normalized Maximum Transient Thermal Impedance

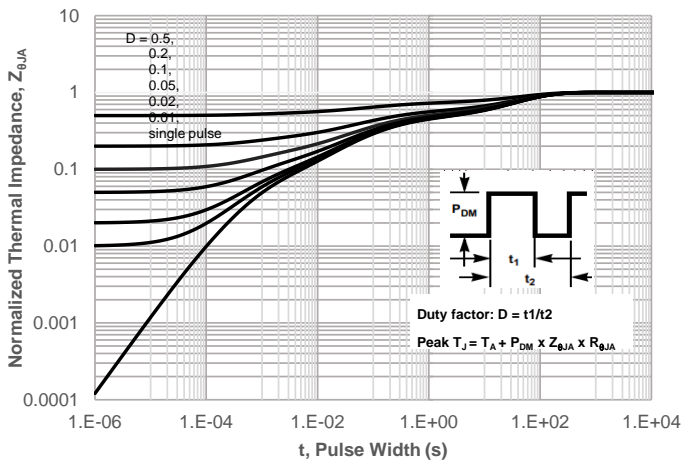
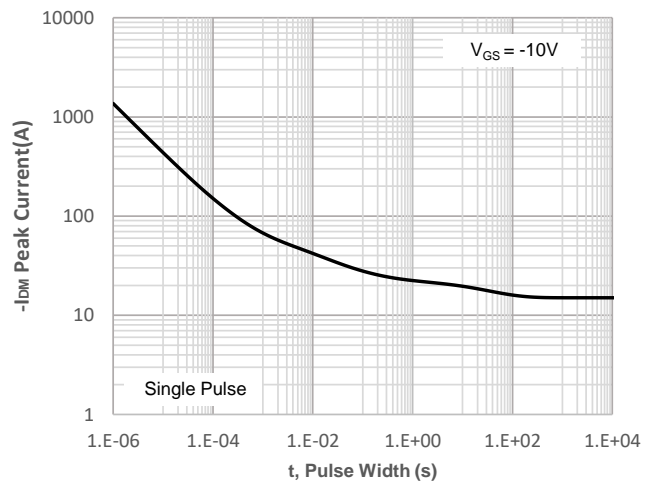


Figure 12: Peak Current Capacity



Test Circuit

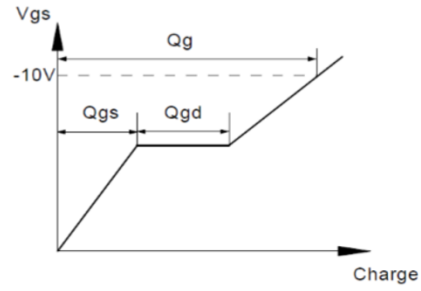
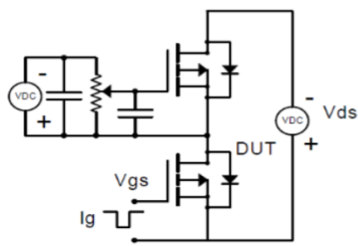


Figure 1: Gate Charge Test Circuit & Waveform

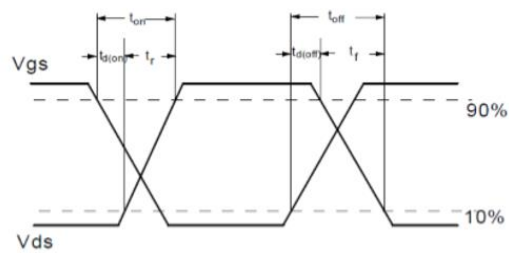
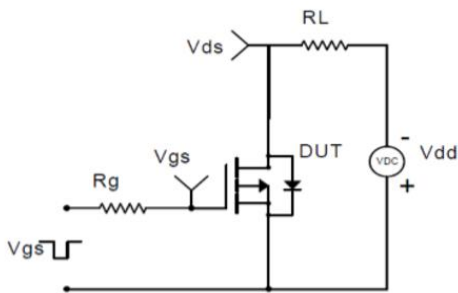


Figure 2: Resistive Switching Test Circuit & Waveform

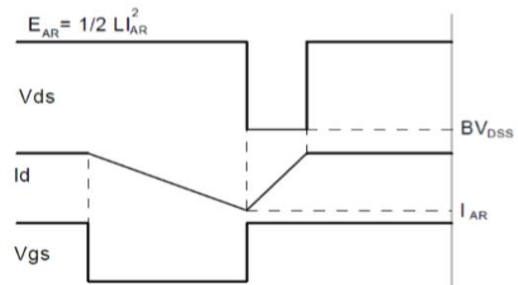
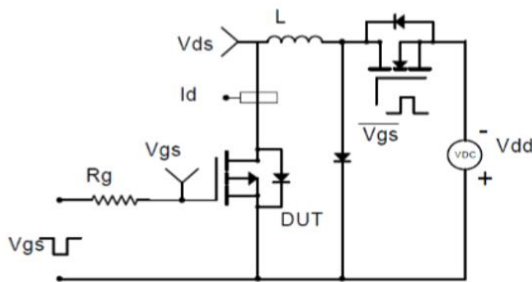


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

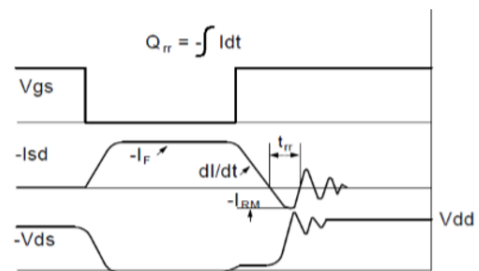
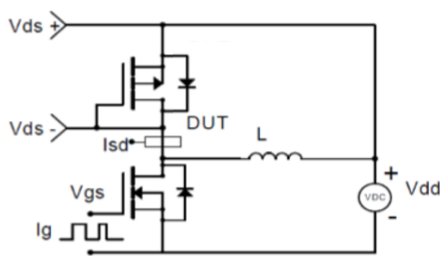
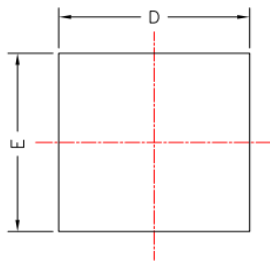


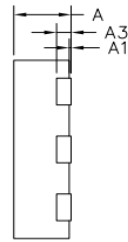
Figure 4: Diode Recovery Test Circuit & Waveform



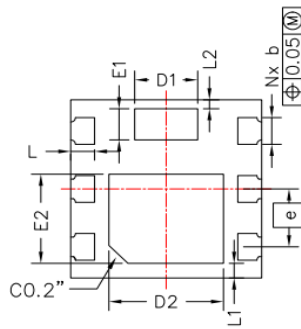
Package Mechanical Data(DFN2020-6L)



Top View



Side View



Bottom View

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.195	0.203	0.211	0.008	0.008	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65BSC			0.026 BSC		
D	1.900	2.000	2.100	0.075	0.079	0.083
E	1.900	2.000	2.100	0.075	0.079	0.083
D1	0.560	0.660	0.760	0.022	0.026	0.030
E1	0.250	0.350	0.450	0.010	0.014	0.018
D2	1.100	1.200	1.300	0.043	0.047	0.051
E2	0.900	1.000	1.100	0.035	0.039	0.043
L	0.150	0.250	0.350	0.006	0.010	0.014
L1	0.065	0.165	0.265	0.003	0.006	0.010
L2	0.000	0.100	0.200	0.000	0.004	0.008

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.
Copyright ©2023 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.