

Description

JMT N-channel Enhancement Mode Power MOSFET

Features

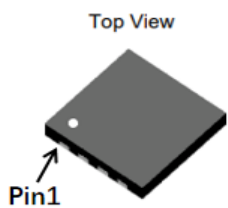
- 30V, 100A
 $R_{DS(ON)} < 3.0m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 4.7m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

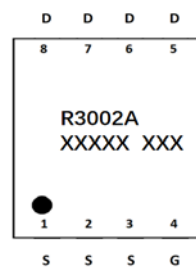
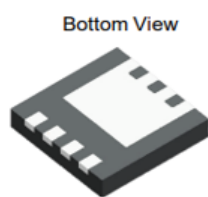
- Load Switch
- PWM Application
- Power Management



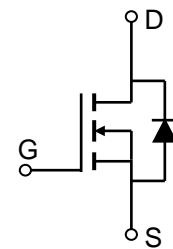
100% UIS TESTED!
100% ΔVds TESTED!



DFN3333-8L Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
R3002A	JMTR3002A	TAPING	DFN3333-8L	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	100
		$T_C = 100^\circ C$	63
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	256	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$ 42	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	38	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 30V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.3	1.9	2.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = 10V, I _D = 30A	-	2.3	3.0	mΩ
		V _{GS} = 4.5V, I _D = 20A	-	3.6	4.7	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz	-	5065	-	pF
C _{oss}	Output Capacitance		-	574	-	pF
C _{rss}	Reverse Transfer Capacitance		-	472	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 10V V _{DS} = 15V, I _D = 30A	-	97	-	nC
Q _{gs}	Gate Source Charge		-	20	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	23	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 10V, V _{DD} = 15V I _D = 30A, R _{GEN} = 3Ω	-	16	-	ns
t _r	Turn-On Rise Time		-	30	-	ns
t _{d(off)}	Turn-Off DelayTime		-	54	-	ns
t _f	Turn-Off Fall Time		-	19	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	100	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	400	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = 30A, di/dt = 100A/us	-	23	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	14	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25C, V_{DD}=15V, V_G=10V, R_G=25ohm, L=0.5mH, I_{AS}=32A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

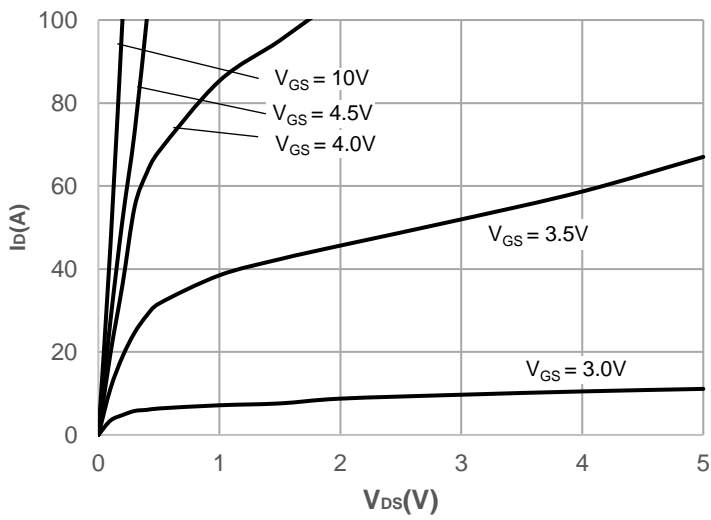


Figure 2: Typical Transfer Characteristics

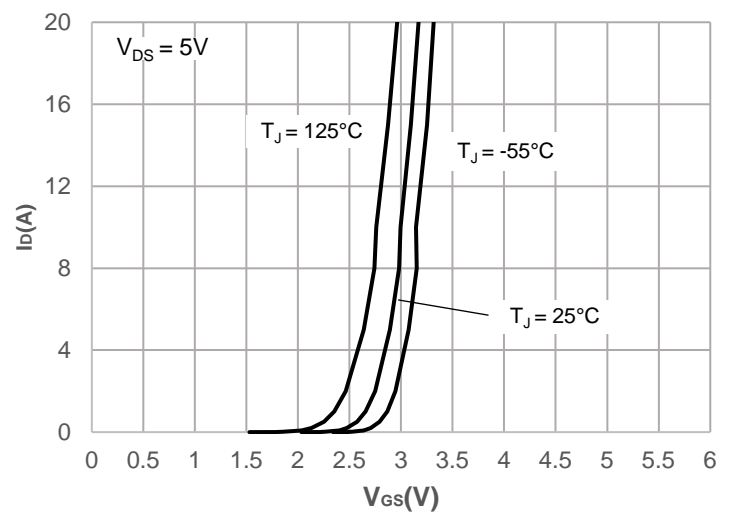


Figure 3: On-resistance vs. Drain Current

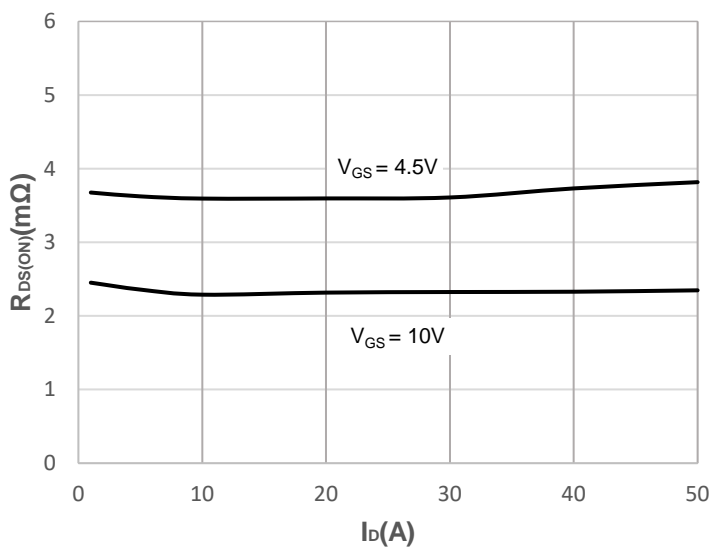


Figure 4: Body Diode Characteristics

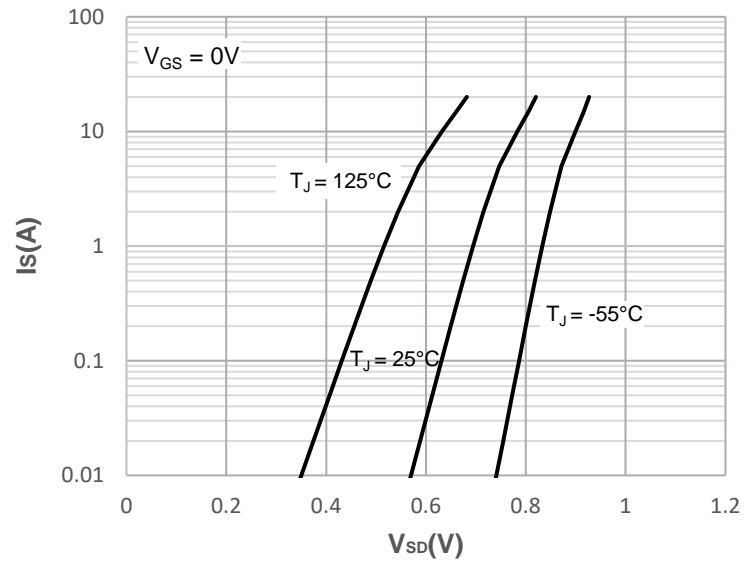


Figure 5: Gate Charge Characteristics

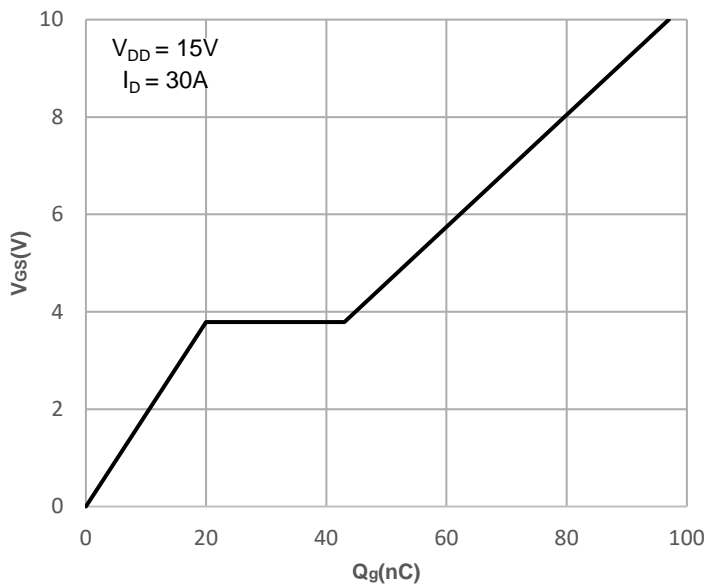
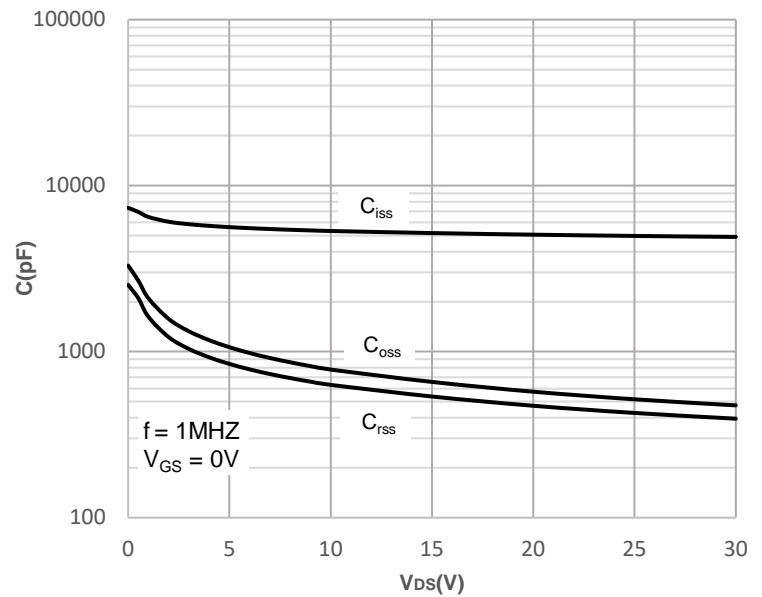


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

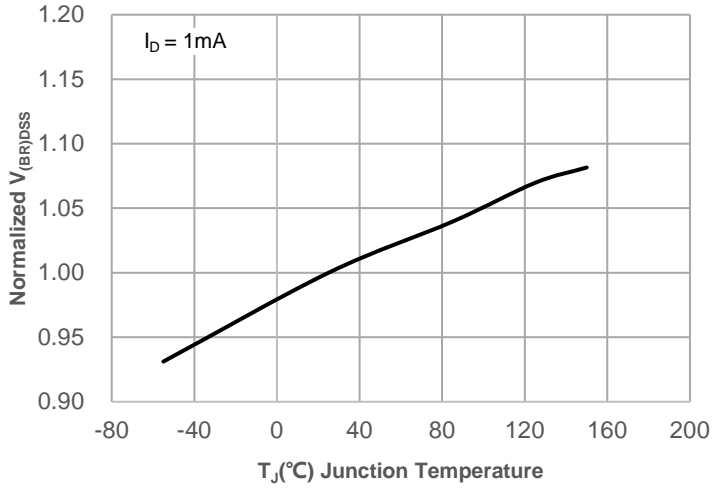


Figure 8: Normalized on Resistance vs. Junction Temperature

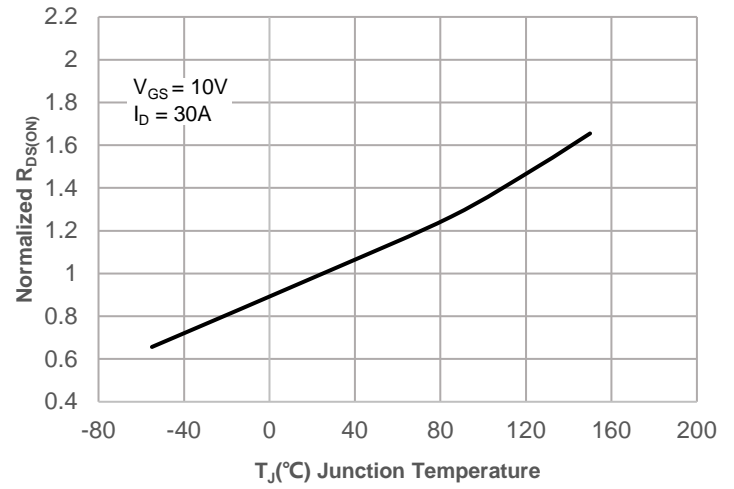


Figure 9: Maximum Safe Operating Area

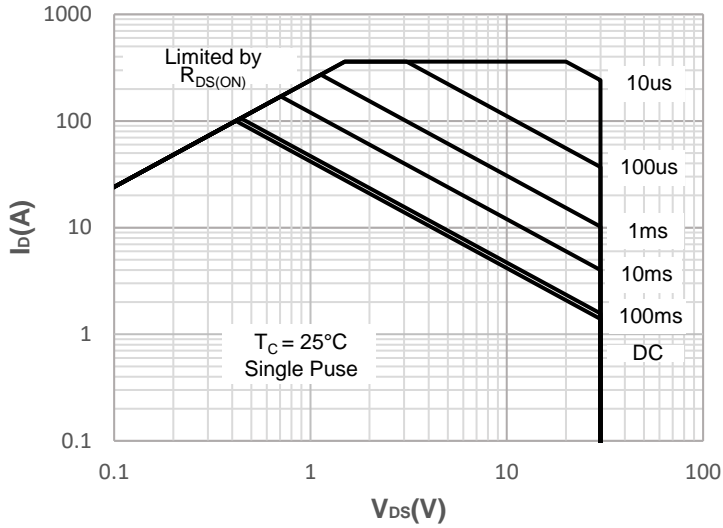


Figure 10: Maximum Continuous Driian Current vs. Case Temperature

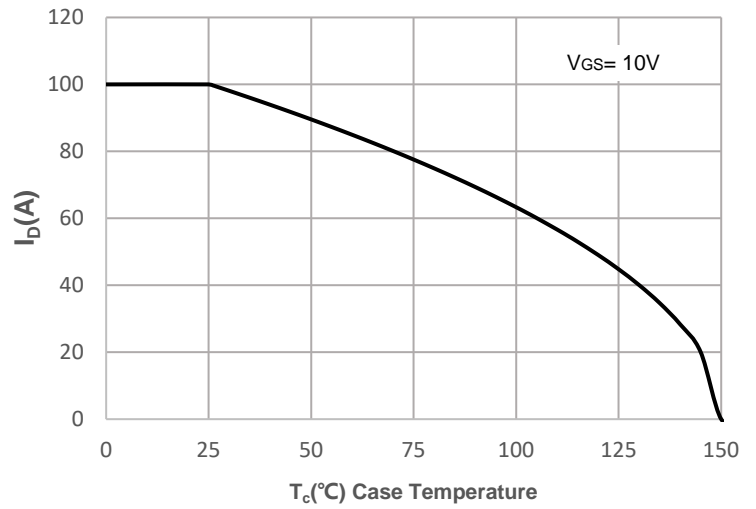


Figure 11: Normalized Maximum Transient Thermal Impedance

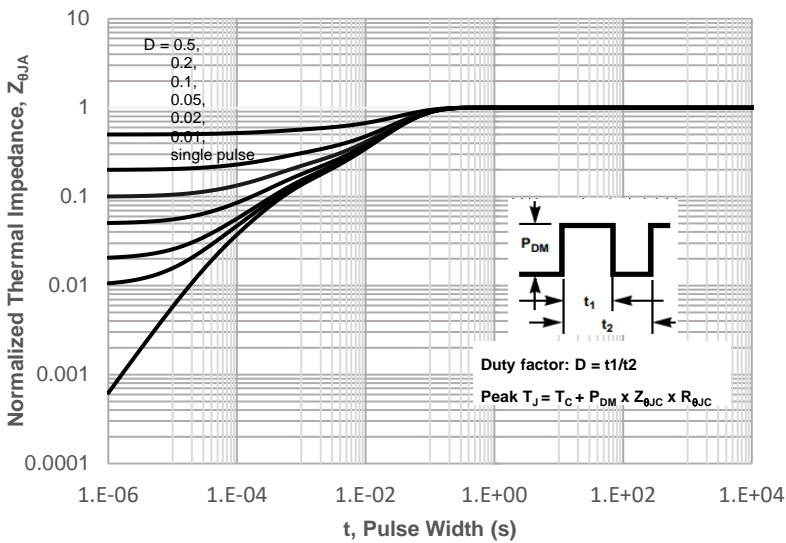
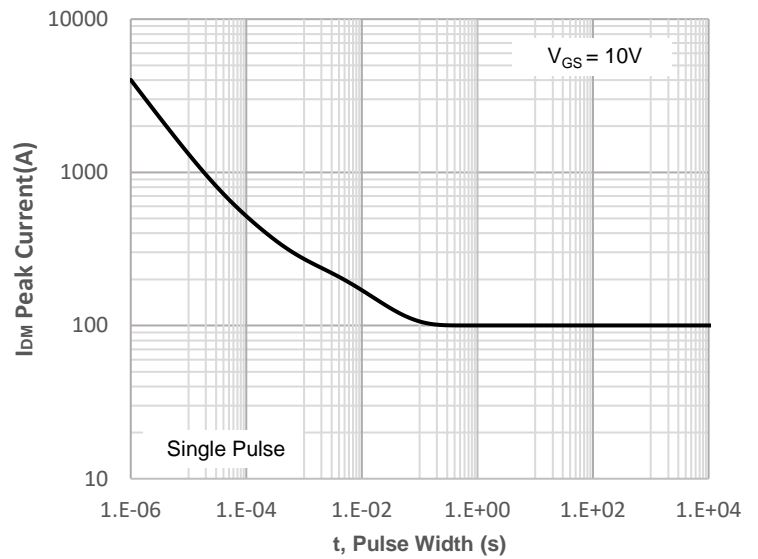


Figure 12: Peak Current Capacity



Test Circuit

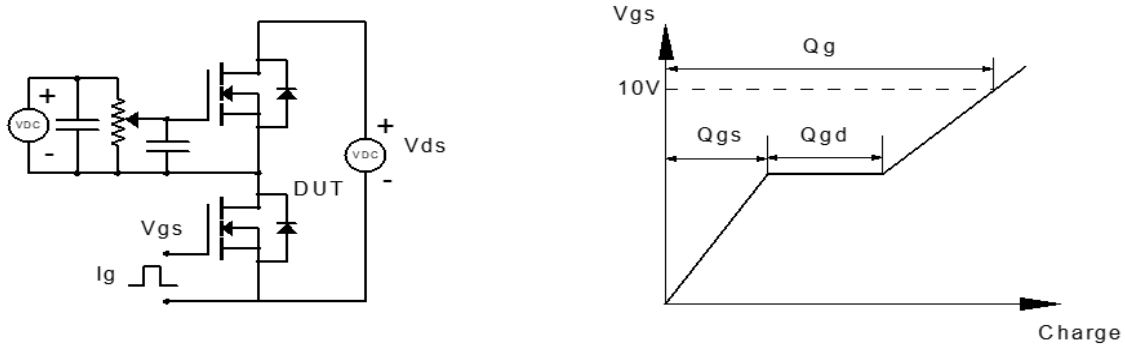


Figure 1: Gate Charge Test Circuit & Waveform

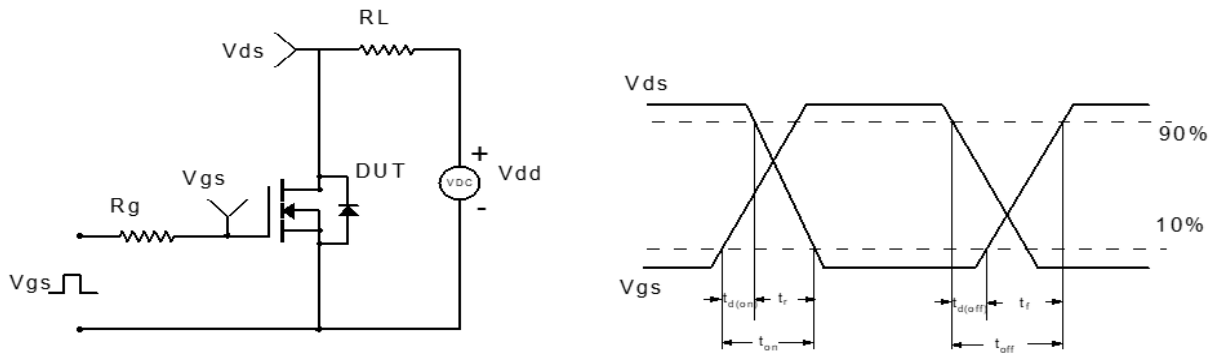


Figure 2: Resistive Switching Test Circuit & Waveform

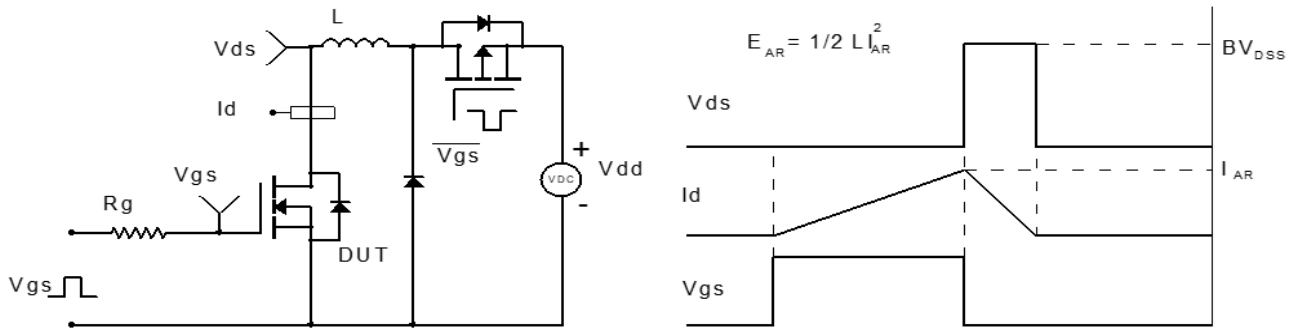


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

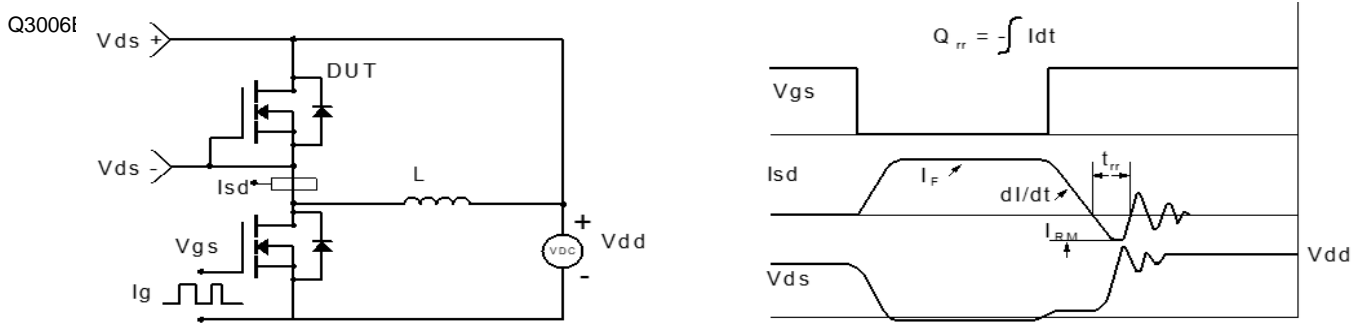
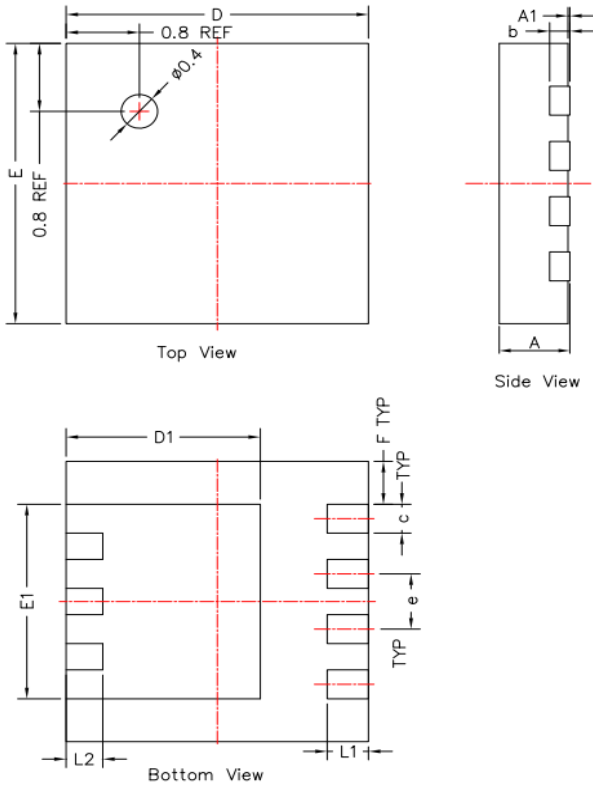


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(DFN3333-8L)



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	#VALUE!	----	0.002
b	0.216 REF			0.0085 REF		
c	0.290	0.340	0.390	0.011	0.013	0.015
e	0.65 BSC			0.026 BSC		
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	2.020	2.120	2.220	0.080	0.083	0.087
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	2.190	2.290	2.390	0.086	0.090	0.094
F	0.405	0.505	0.605	0.016	0.020	0.024
L1	0.350	0.450	0.550	0.01	0.02	0.02
L2	0.300	0.400	0.500	0.01	0.02	0.02

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