



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

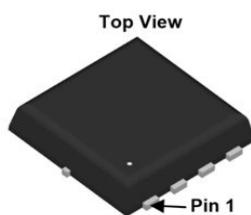
- 40V, 20A
- $R_{DS(ON)} < 19.2\text{m}\Omega @ V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 25.4\text{m}\Omega @ V_{GS} = 4.5\text{V}$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

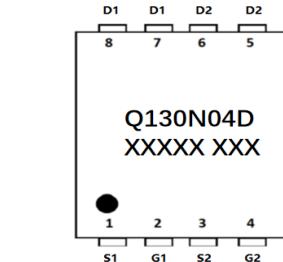
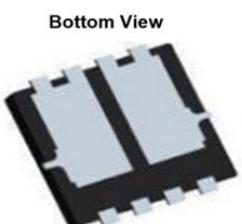
- Load Switch
- PWM Application
- Power Management



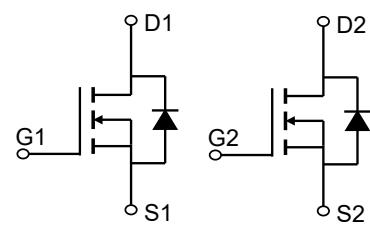
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3x3-8L-D



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
Q130N04D	JMTQ130N04D	TAPING	PDFN3x3-8L-D	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ\text{C}$	20	A
		13	
I_{DM}	Pulsed Drain Current ⁽¹⁾	80	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	30	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	50	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	61	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



JMTQ130N04D

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.3	2	2.3	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	14.8	19.2	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-	19.5	25.4	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 20\text{V}, f = 1\text{MHz}$	-	1342	-	pF
C_{oss}	Output Capacitance		-	87	-	pF
C_{rss}	Reverse Transfer Capacitance		-	72	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 20\text{V}, I_D = 10\text{A}$	-	26	-	nC
Q_{gs}	Gate Source Charge		-	6	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 20\text{V}$ $I_D = 10\text{A}, R_{\text{GEN}} = 3\Omega$	-	7	-	ns
t_r	Turn-On Rise Time		-	11	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Turn-Off Fall Time		-	5	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	20	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	80	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 20\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 10\text{A}, di/dt = 100\text{A/us}$	-	10	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	6	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=20\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=0.5\text{mH}$, $I_{AS}=11\text{A}$ 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

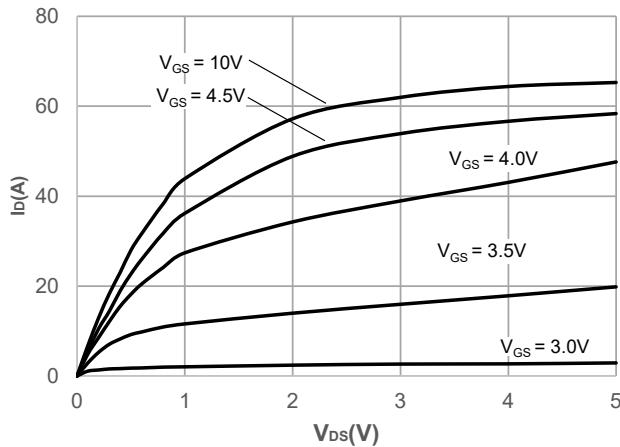


Figure 2: Typical Transfer Characteristics

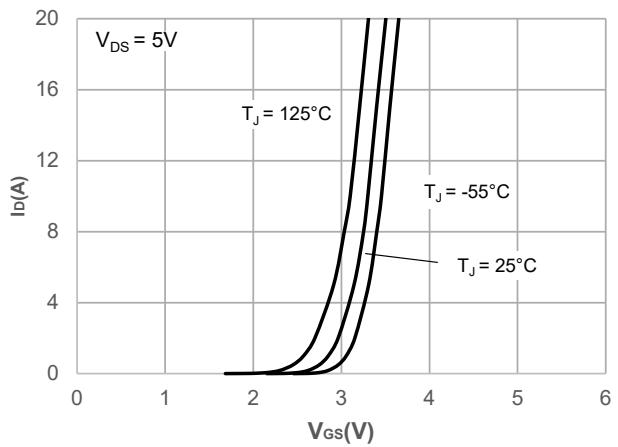


Figure 3: On-resistance vs. Drain Current

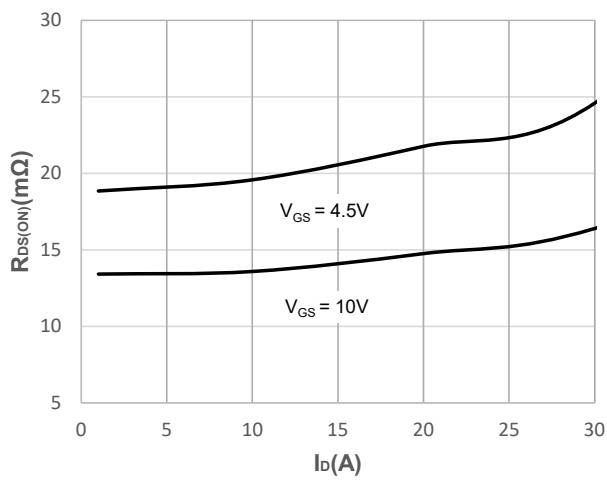


Figure 4: Body Diode Characteristics

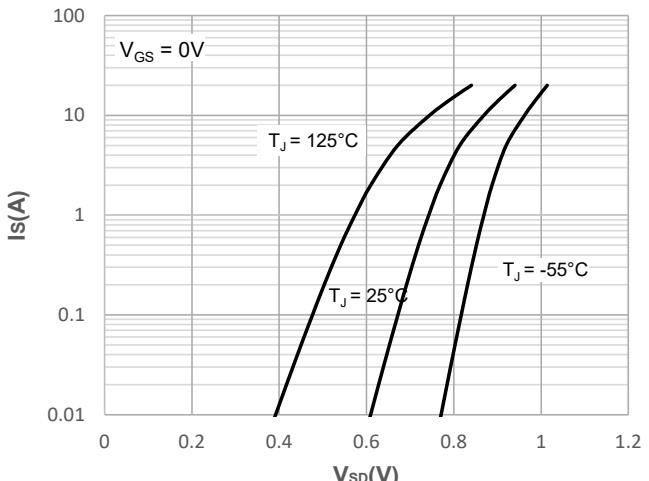


Figure 5: Gate Charge Characteristics

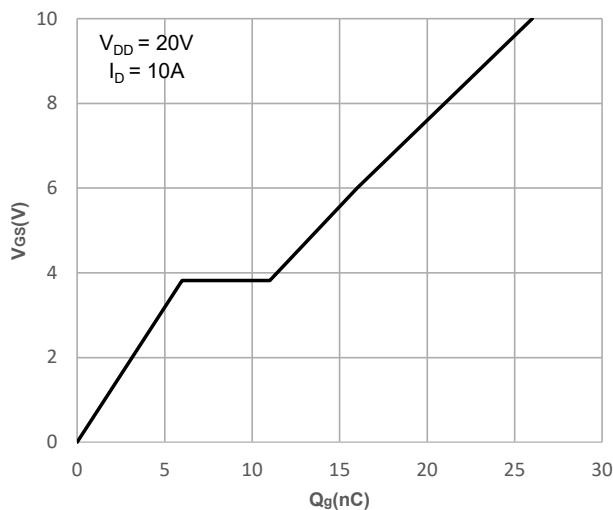
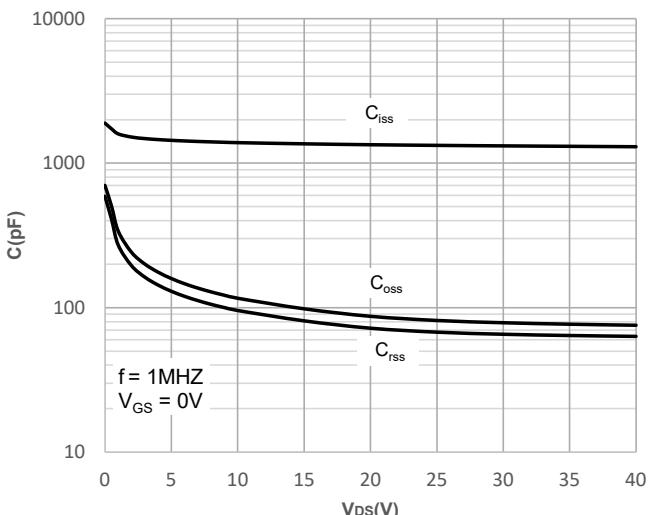


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

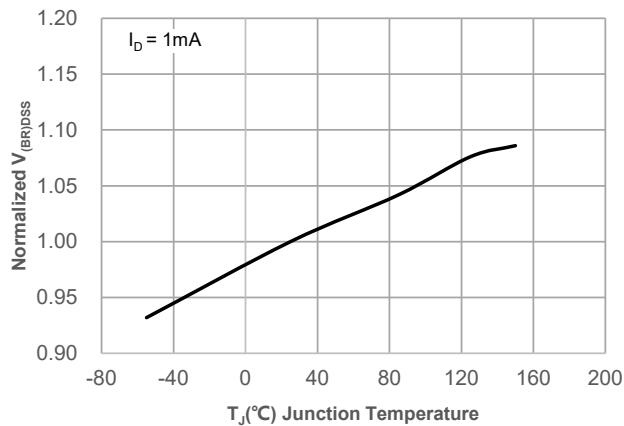


Figure 8: Normalized on Resistance vs. Junction Temperature

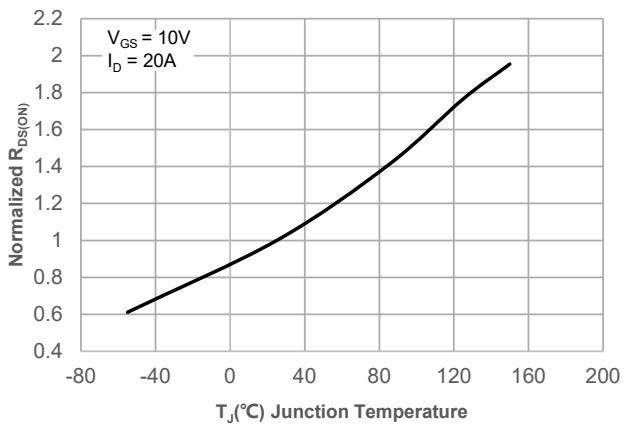


Figure 9: Maximum Safe Operating Area

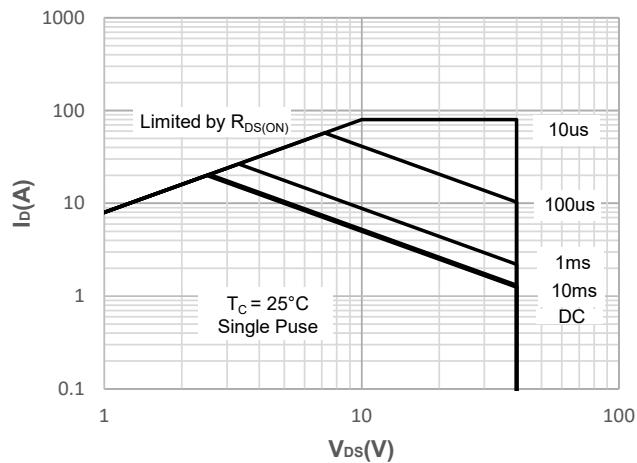


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

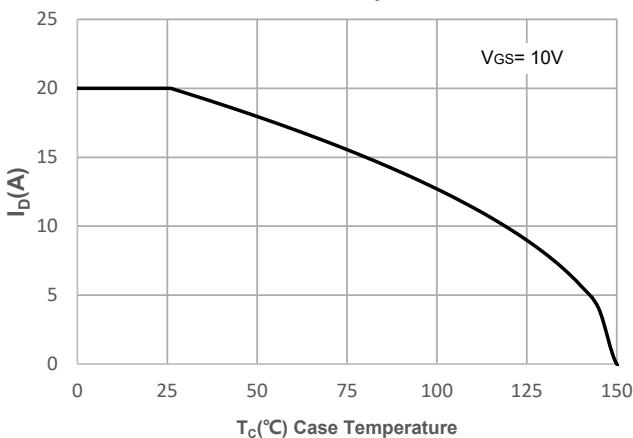


Figure 11: Normalized Maximum Transient Thermal Impedance

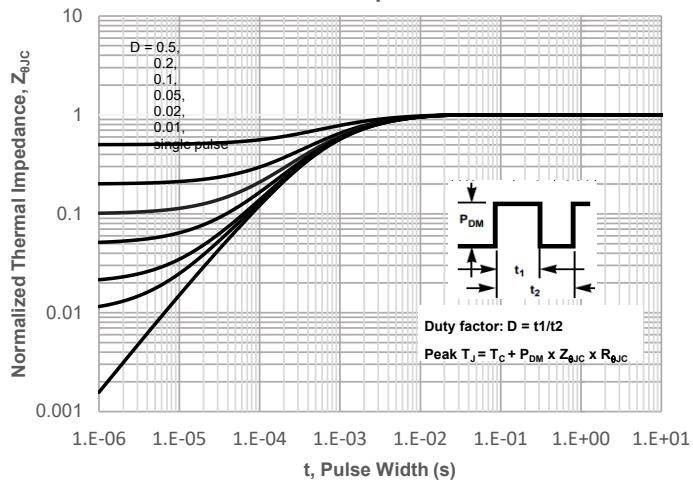
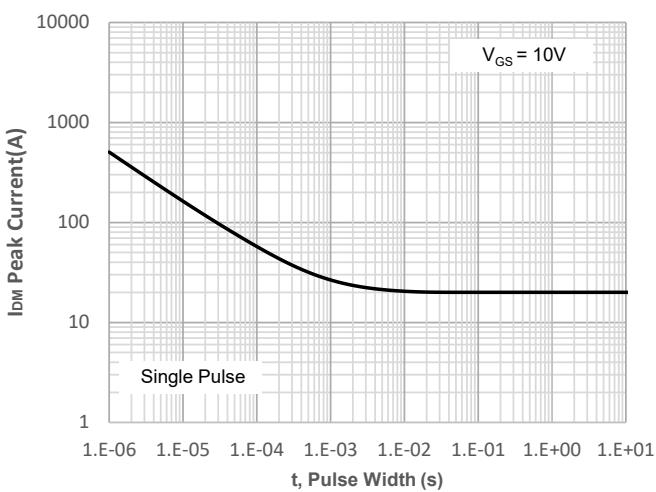


Figure 12: Peak Current Capacity



Test Circuit

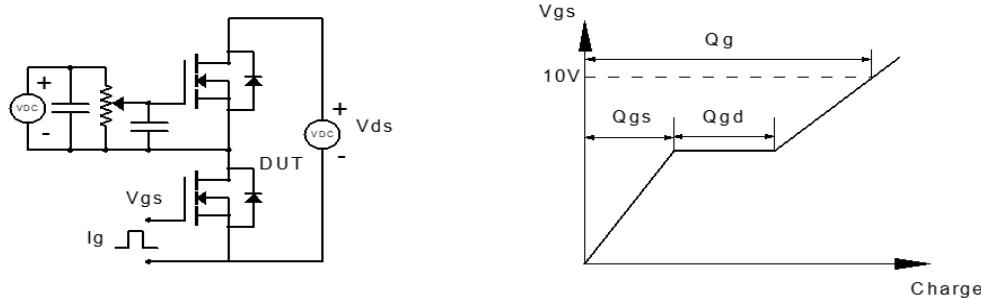


Figure 1: Gate Charge Test Circuit & Waveform

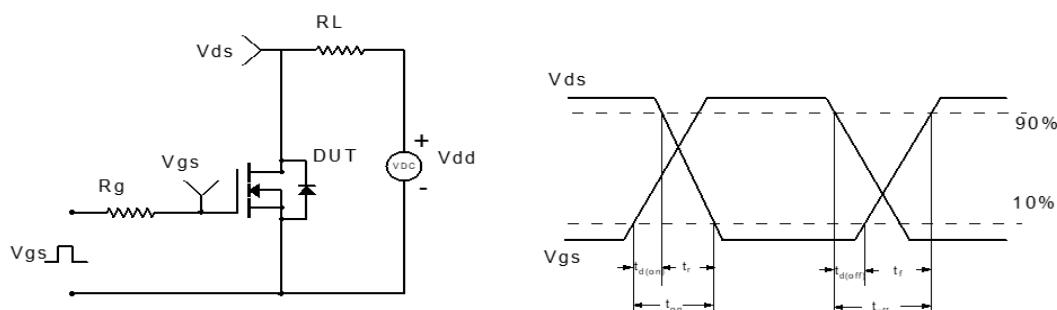


Figure 2: Resistive Switching Test Circuit & Waveform

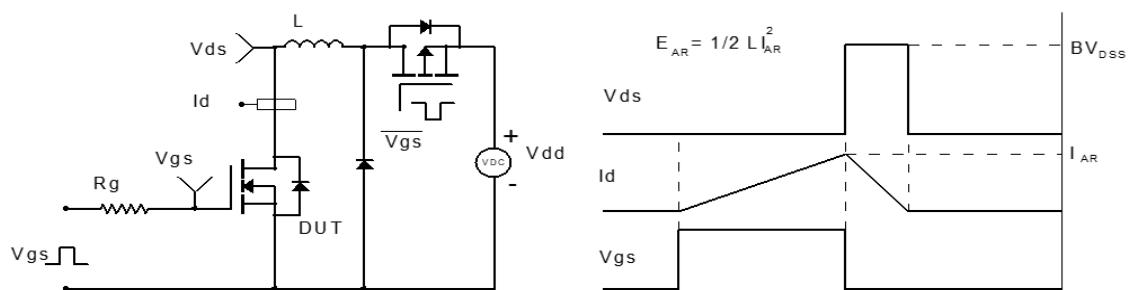


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

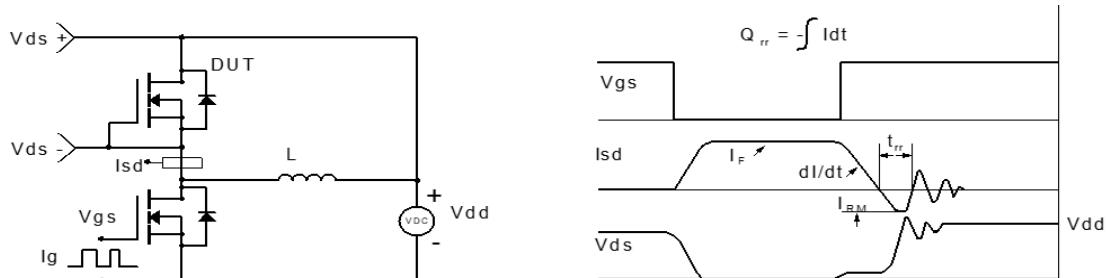
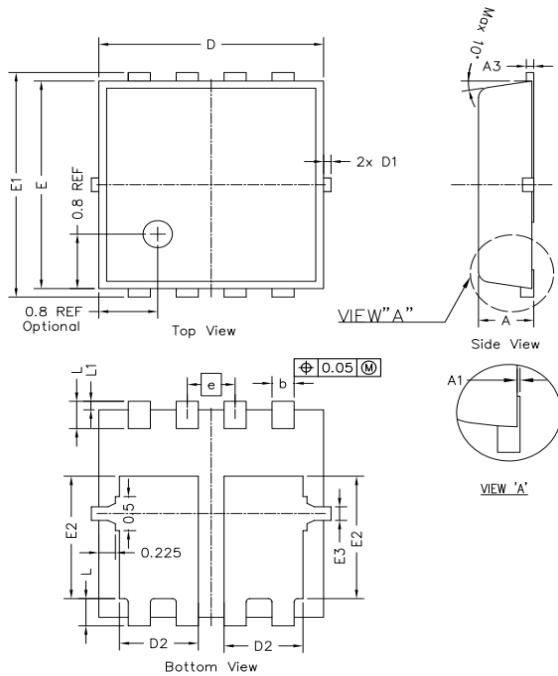


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN3x3-8L-D)



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.144	0.152	0.202	0.006	0.006	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
E	2.950	3.050	3.150	0.116	0.120	0.124
D1	---	---	0.125	----	----	0.005
E1	3.200	3.300	3.400	0.126	0.130	0.134
D2	0.970	1.070	1.170	0.038	0.042	0.046
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	0.150	0.200	0.250	0.006	0.008	0.010
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.075	0.125	0.175	0.003	0.005	0.007

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