JMTK4005A

Description

JMT N-channel Enhancement Mode Power MOSFET

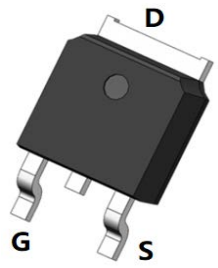
Features

- 40V, 80A
  $R_{DS(ON)}$ < 4.9mΩ @ V_{GS} = 10V
  $R_{DS(ON)}$ < 7.4mΩ @ V_{GS} = 4.5V
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

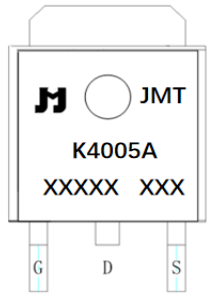
Applications

- Load Switch
- PWM Application
- Power Management

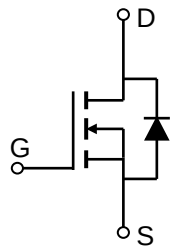
100% UIS TESTED!
100% ΔVds TESTED!



TO-252-3L(DPAK) Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
JMTK4005A	JMTK4005A	TAPING	TO-252-3L	13"	2500	25000

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Units
V_{DS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current	T_C = 25°C	80	A
		T_C = 100°C	50	
I_{DM}	Pulsed Drain Current (1)		320	A
E_{AS}	Single Pulsed Avalanche Energy (2)		156	mJ
P_D	Power Dissipation	T_C = 25°C	142	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (3)		31	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.88	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40V, V_{GS} = 0V	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.3	1.9	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(4)	V_{GS} = 10V, I_D = 30A	-	3.8	4.9	mΩ
		V_{GS} = 4.5V, I_D = 20A	-	5.7	7.4	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	-	3778	-	pF
C_{oss}	Output Capacitance		-	267	-	pF
C_{rss}	Reverse Transfer Capacitance		-	224	-	pF
Q_g	Total Gate Charge	V_{GS} = 0 to 10V, V_{DS} = 20V, I_D = 30A	-	73	-	nC
Q_{gs}	Gate Source Charge		-	15	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	16	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = 10V, V_{DD} = 20V, I_D= 30A, R_{GEN} = 3Ω	-	12	-	ns
t_r	Turn-On Rise Time		-	29	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	60	-	ns
t_f	Turn-Off Fall Time		-	16	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	80	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	320	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = 30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F = 20A, di/dt = 100A/us	-	16	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	10	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting T_J=25C, V_{DD}=20V, V_G=10V, R_G=25ohm, L=0.5mH, I_{AS}=25A
3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

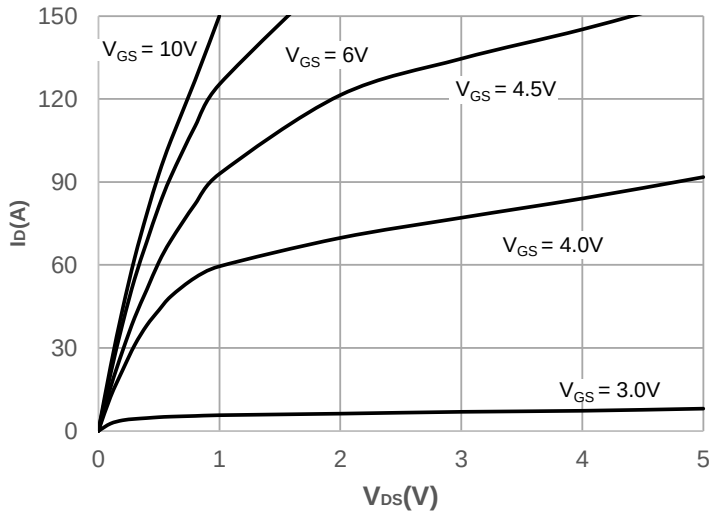


Figure 2: Typical Transfer Characteristics

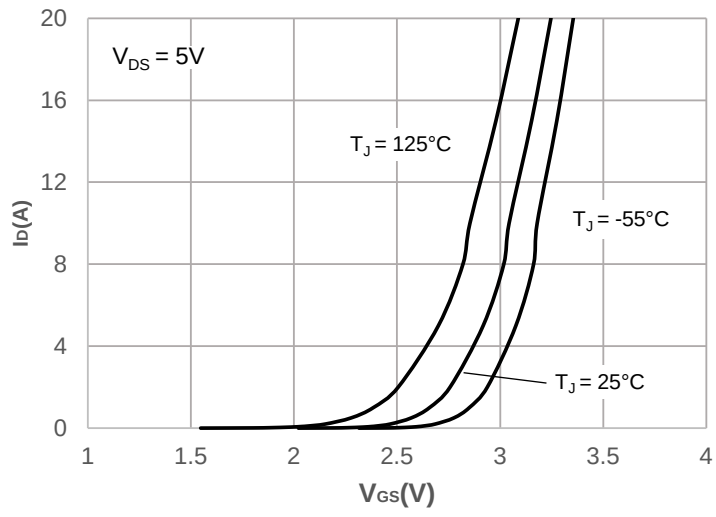


Figure 3: On-resistance vs. Drain Current

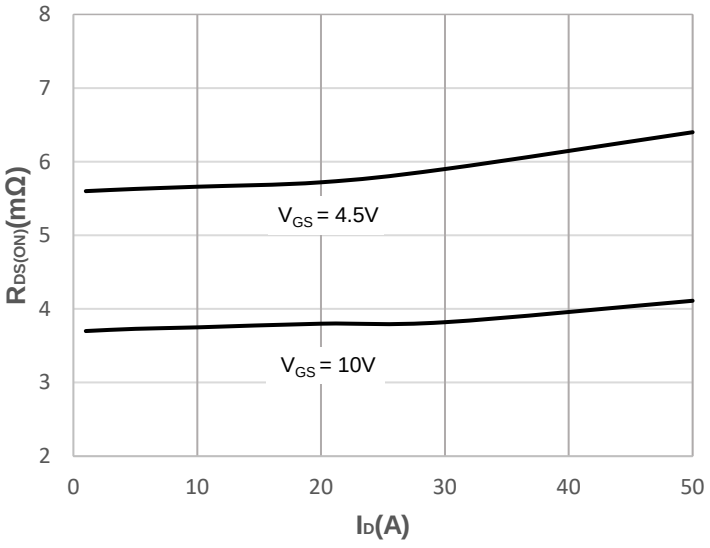


Figure 4: Body Diode Characteristics

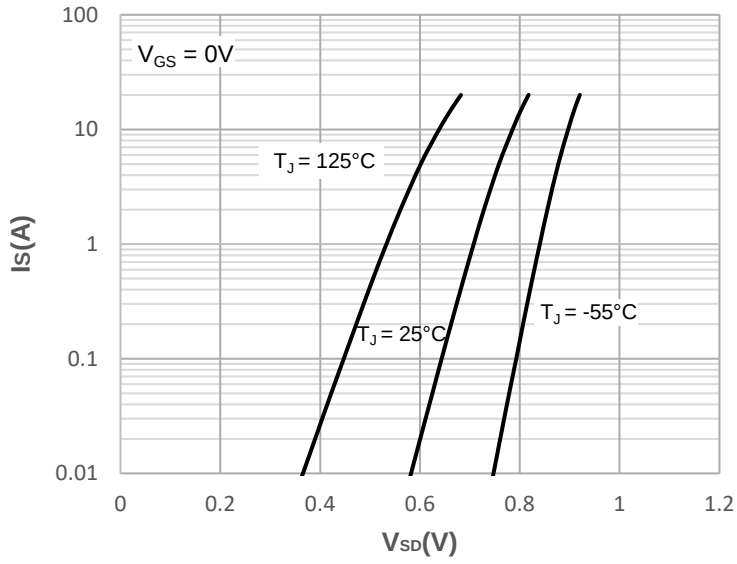


Figure 5: Gate Charge Characteristics

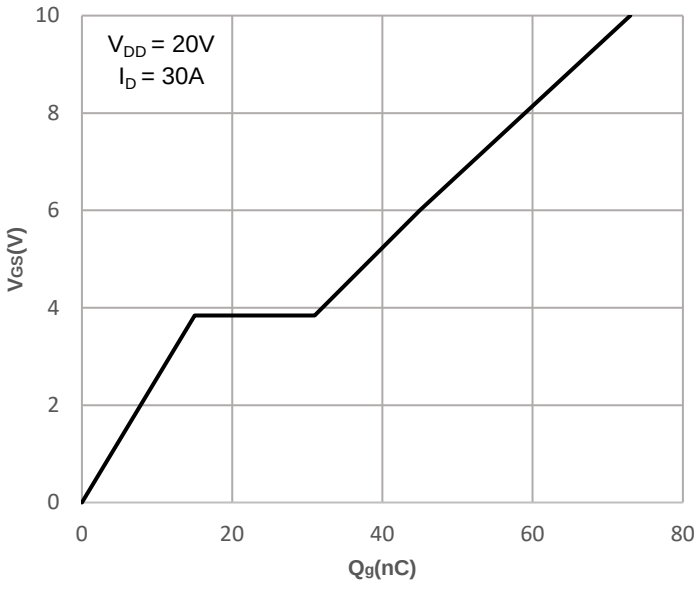
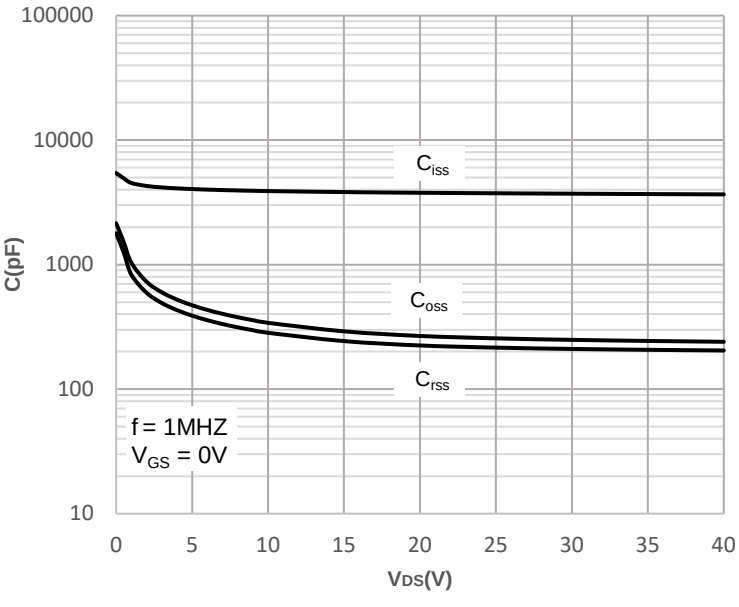


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

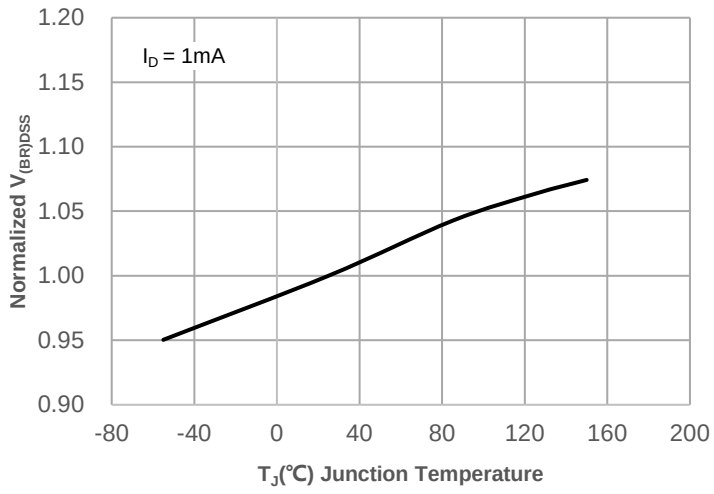


Figure 8: Normalized on Resistance vs. Junction Temperature

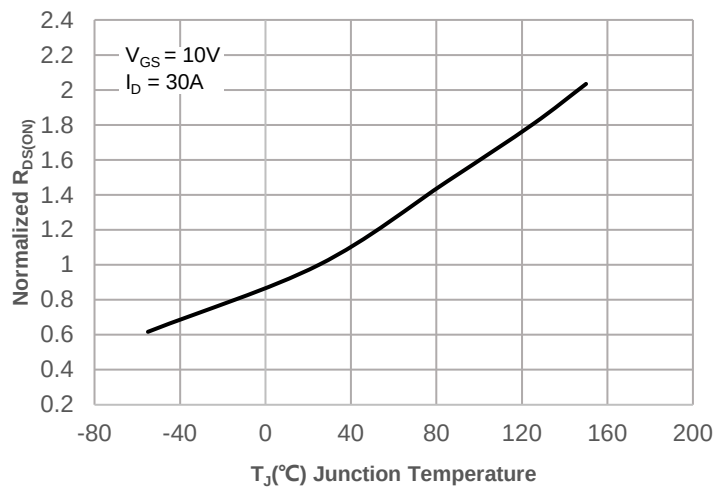


Figure 9: Maximum Safe Operating Area

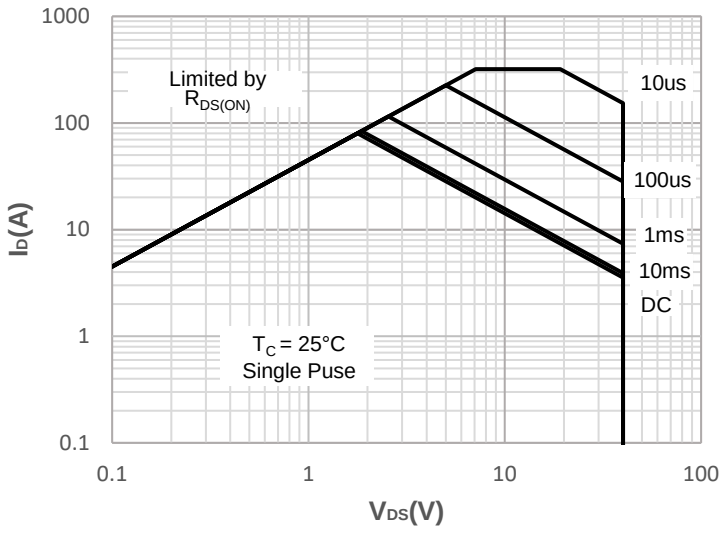


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

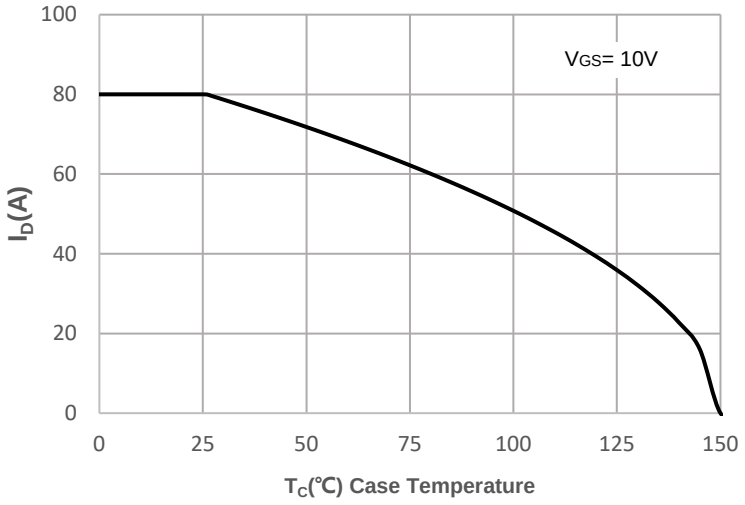


Figure 11: Normalized Maximum Transient Thermal Impedance

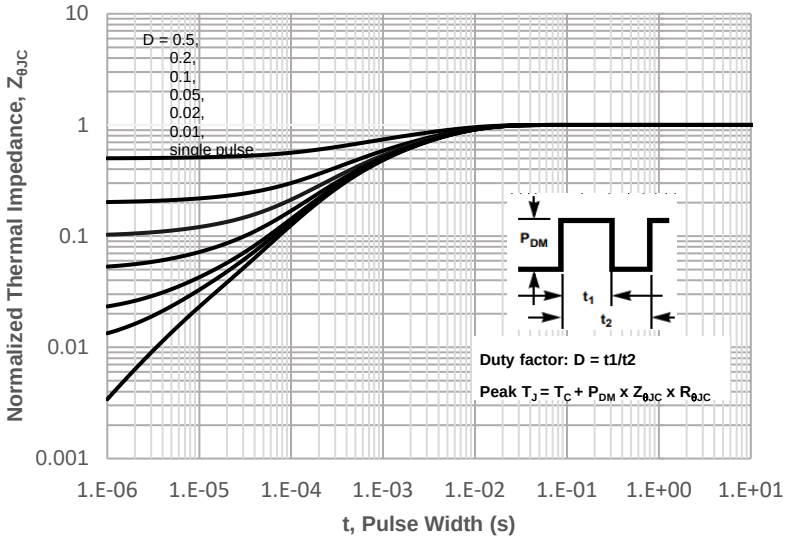
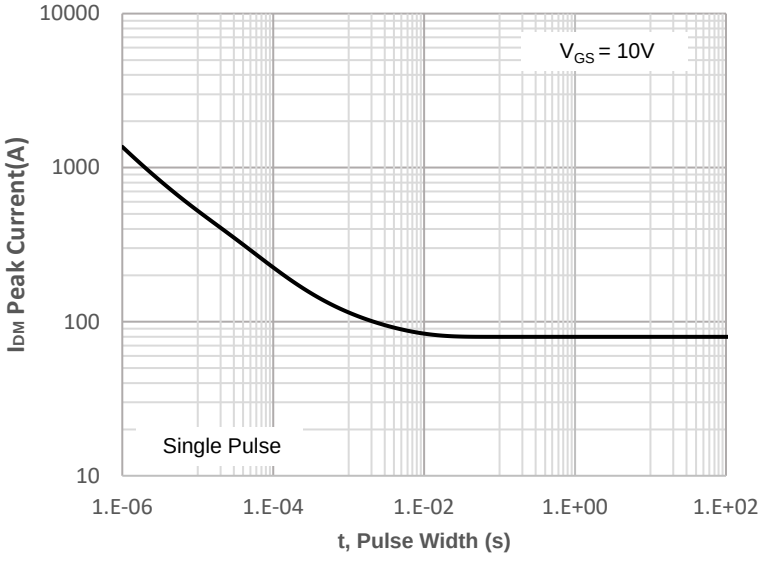


Figure 12: Peak Current Capacity



Test Circuit

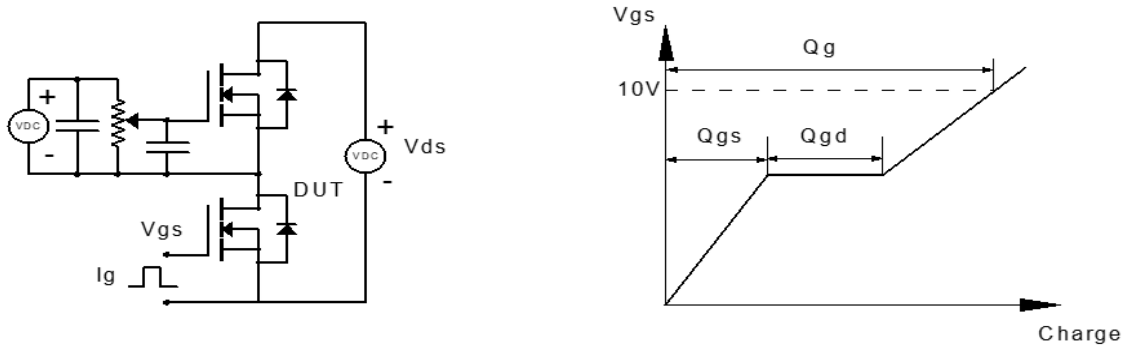


Figure 1: Gate Charge Test Circuit & Waveform

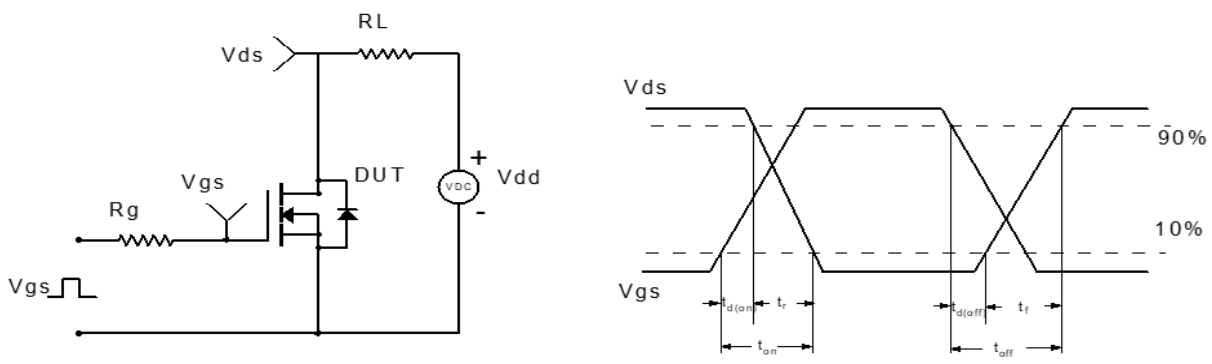


Figure 2: Resistive Switching Test Circuit & Waveform

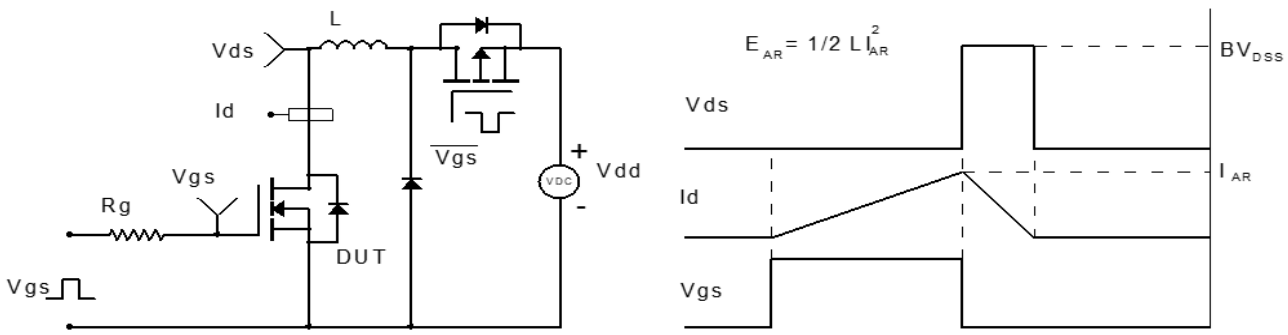


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

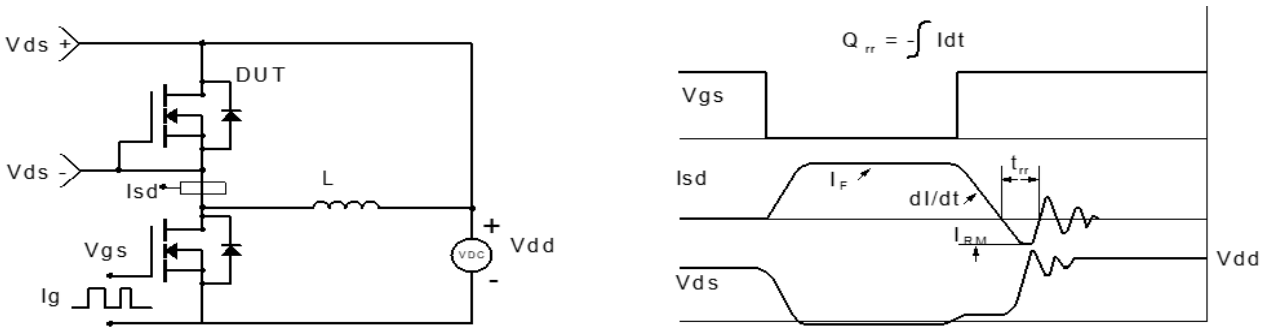
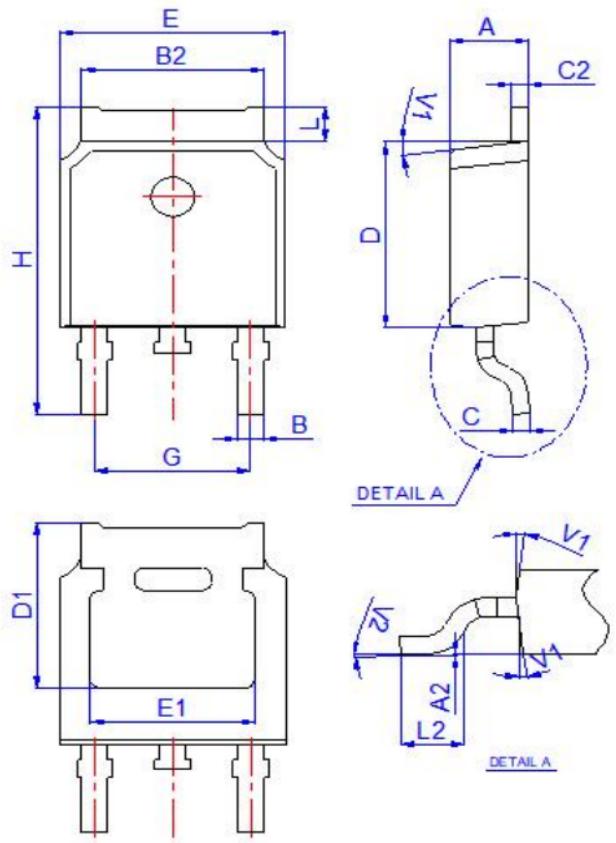


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-252-3L)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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