



## Description

### JMT N-channel Enhancement Mode Power MOSFET

#### Features

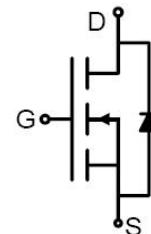
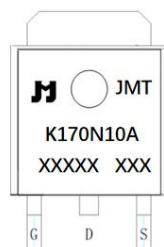
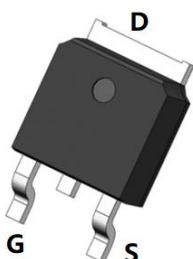
- 100V,59A
- $R_{DS(ON)} < 20m\Omega$  @  $V_{GS} = 10V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

- Load Switch
- PWM Application
- Power management



100% UIS TESTED!  
100%  $\Delta V_{ds}$  TESTED!



TO-252-3L(DPAK) top view

Marking and pin Assignment

Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner BOX (PCS)	Per Carton (PCS)
JMTK170N10A	JMTK170N10A	TAPING	TO-252-3L	13inch	2500	25000

## Absolute Maximum Ratings ( $T_c = 25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
$V_{DSS}$	Drain-Source Voltage		100	V
$V_{GSS}$	Gate-Source Voltage		$\pm 25$	V
$I_D$	Continuous Drain Current	$T_c = 25^\circ C$	59	A
		$T_c = 100^\circ C$	38	A
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>		236	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>		110	mJ
$P_D$	Power Dissipation	$T_c = 25^\circ C$	153	W
$R_{eJC}$	Thermal Resistance, Junction to Case		0.98	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +175	$^\circ C$

**Electrical Characteristics** ( $T_C=25^\circ C$  unless otherwise specified)

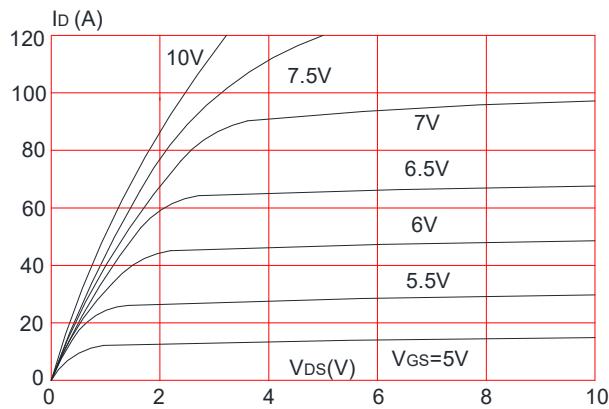
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	$V_{GS}=10V, I_D=30A$	-	15	20	$m\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	5211	-	pF
$C_{oss}$	Output Capacitance		-	232	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	163	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$	-	87	-	nC
$Q_{gs}$	Gate-Source Charge		-	27	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	21	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30V, I_D=2A,$ $R_L=15\Omega, R_{GEN}=2.5\Omega,$ $V_{GS}=10V$	-	18	-	ns
$t_r$	Turn-on Rise Time		-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	50	-	ns
$t_f$	Turn-off Fall Time		-	20	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	59	-	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	236	-	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=59A$	-	-	1.2	V
$trr$	Body Diode Reverse Recovery Time	$T_J = 25^\circ C$ $I_F=28A, dI/dt=100A/\mu s$	-	32	-	ns
$Qrr$	Body Diode Reverse Recovery Charge		-	55	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

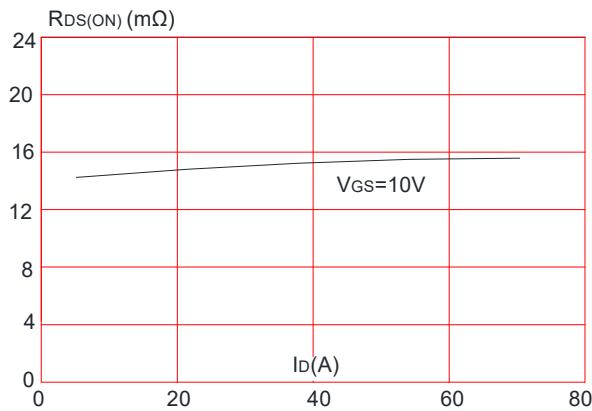
2. EAS condition:  $T_J=25^\circ C$ ,  $V_{DD}=50V$ ,  $V_G=10V$ ,  $L=0.5mH$ ,  $R_G=25\Omega$ ,  $I_{AS}=21A$ 3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$

## Typical Performance Characteristics

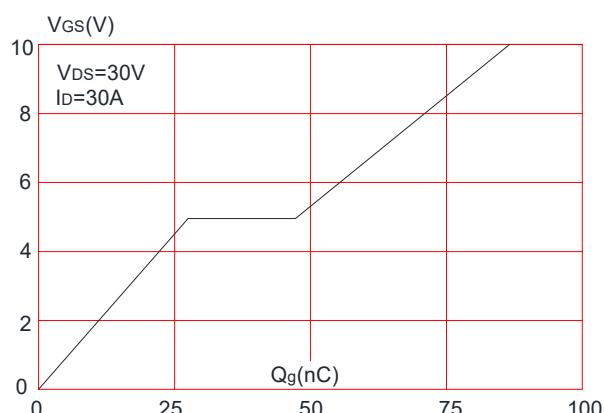
**Figure 1:** Output Characteristics



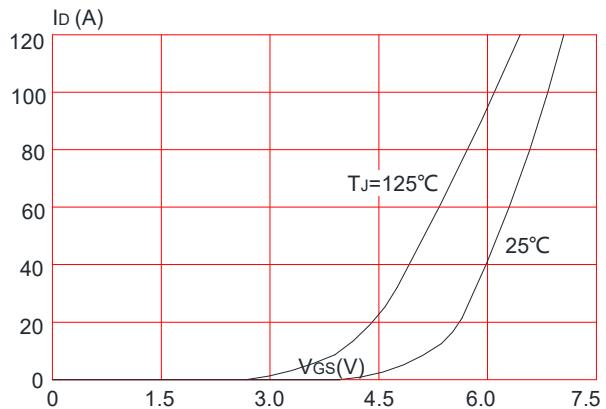
**Figure 3:** On-resistance vs. Drain Current



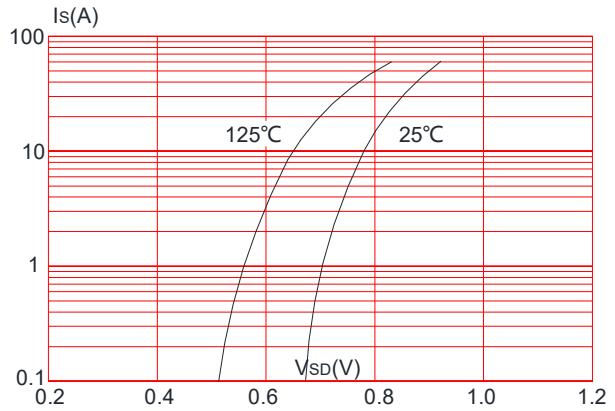
**Figure 5:** Gate Charge Characteristics



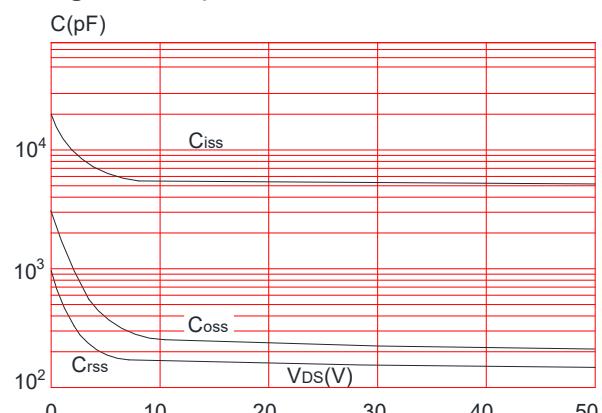
**Figure 2:** Typical Transfer Characteristics



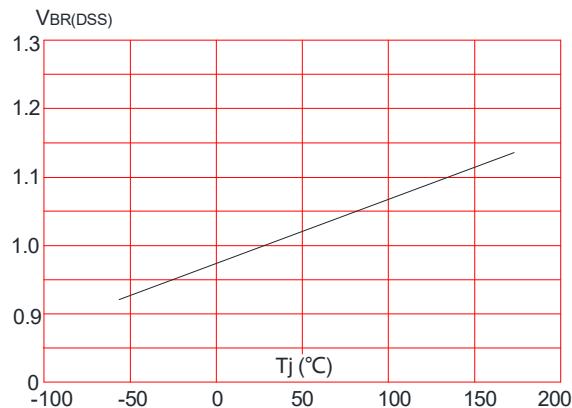
**Figure 4:** Body Diode Characteristics



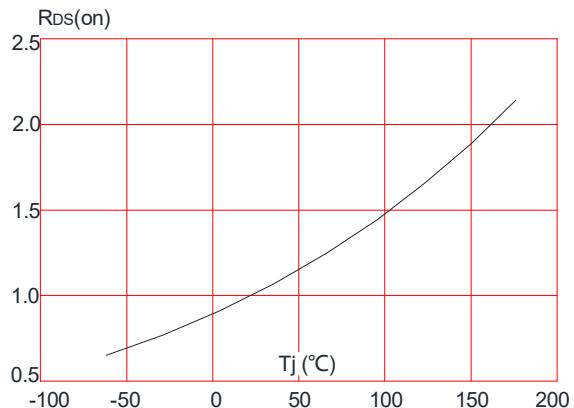
**Figure 6:** Capacitance Characteristics



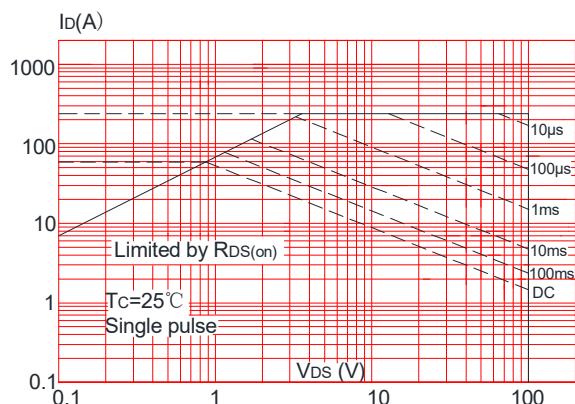
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



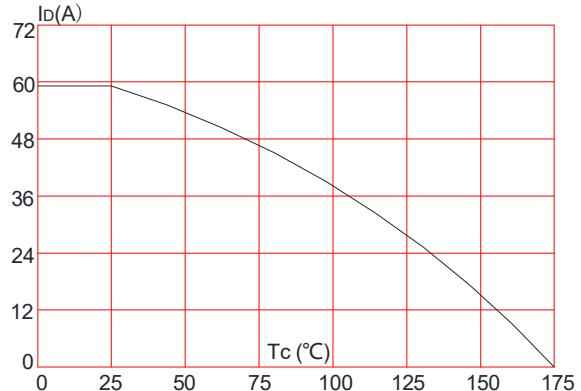
**Figure 8:** Normalized on Resistance vs. Junction Temperature



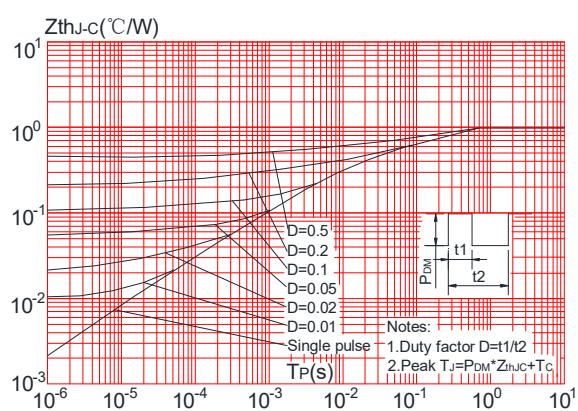
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

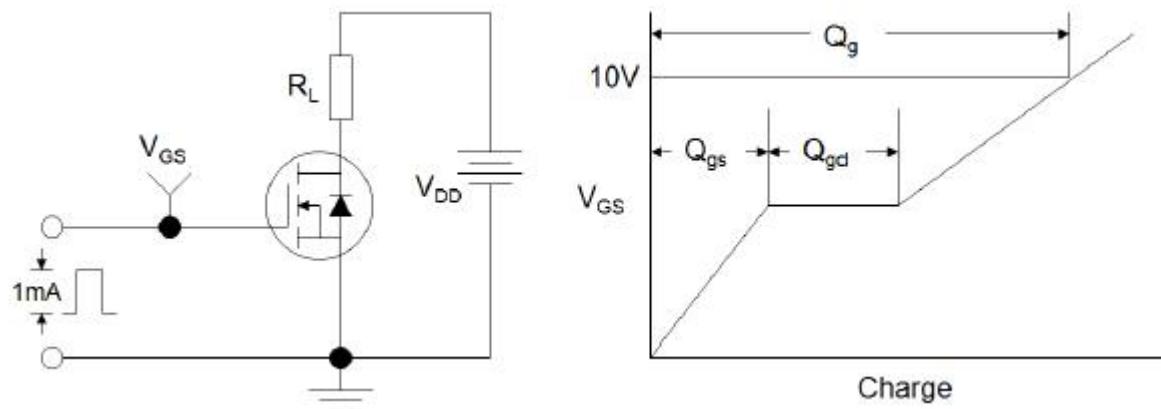


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

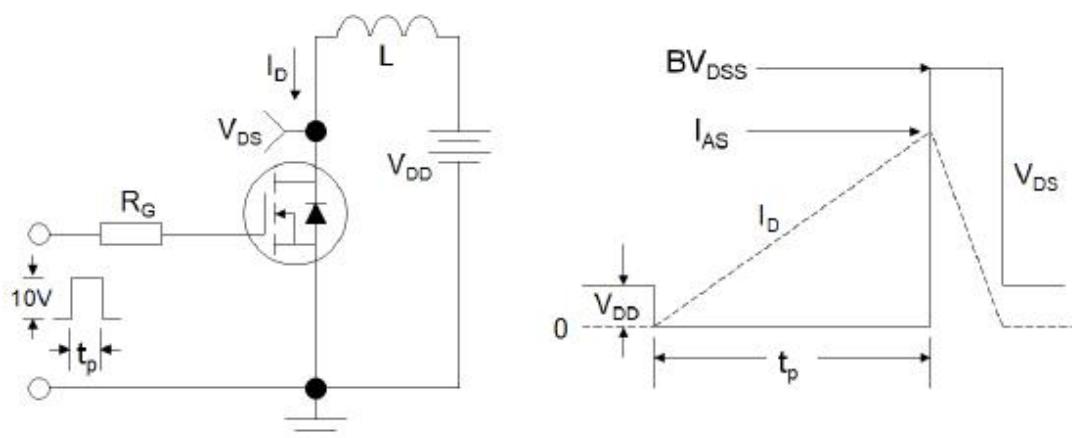
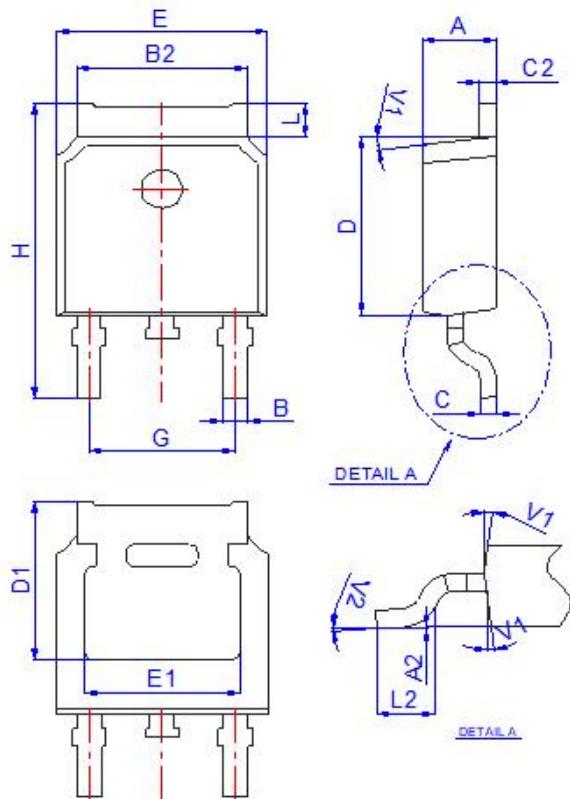


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data-TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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