



Description

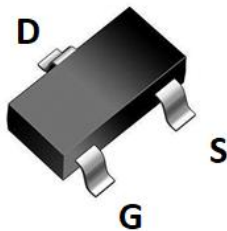
JMT N-channel Enhancement Mode Power MOSFET

Features

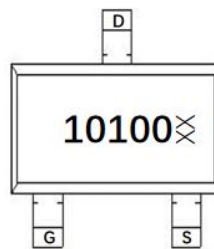
- 100V, 3A
- $R_{DS(ON)} < 115m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 127m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Application

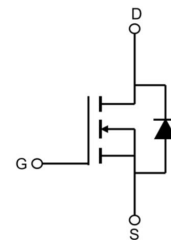
- Load Switch
- PWM Application
- Power Management



SOT-23-3L top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
10100	JMTJ11DN10A	TAPING	SOT-23-3L	7"	3000	120000

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V _{DSS}	Drain-Source Voltage	100	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current	T _A = 25°C	3
		T _A = 100°C	2
I _{DM}	Pulsed Drain Current ^{note1}	12	A
P _D	Power Dissipation	1.38	W
R _{θJA}	Thermal Resistance, Junction to Ambient	90	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>Note2</small>	V _{GS} =10V, I _D =3A	-	92	115	mΩ
		V _{GS} =4.5V, I _D =2A	-	98	127	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	847	-	pF
C _{oss}	Output Capacitance		-	40	-	pF
C _{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q _g	Total Gate Charge	V _{DD} =50V, I _D =2A, V _{GS} =10V	-	20	-	nC
Q _{gs}	Gate-Source Charge		-	2.8	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	4	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =3A, R _{GEN} =1.8Ω, V _{GS} =10V	-	6	-	ns
t _r	Turn-on Rise Time		-	7	-	ns
t _{d(off)}	Turn-off Delay Time		-	21	-	ns
t _f	Turn-off Fall Time		-	3	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =3A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I _F =3A, di/dt=100A/μs	-	15	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	20	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

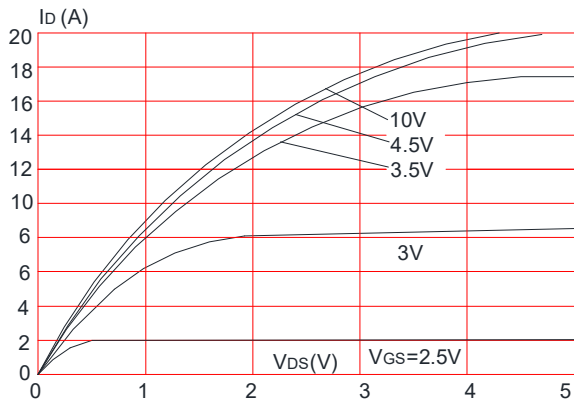


Figure 2: Typical Transfer Characteristics

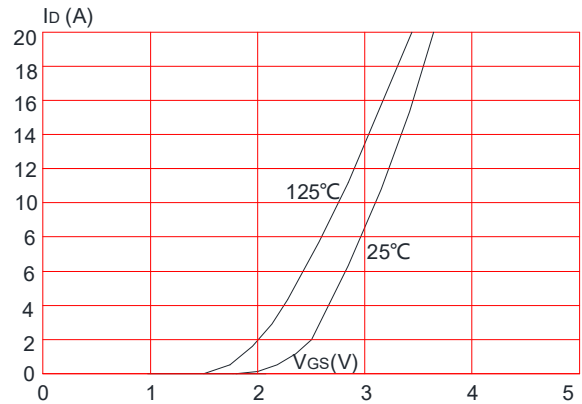


Figure 3: On-resistance vs. Drain Current

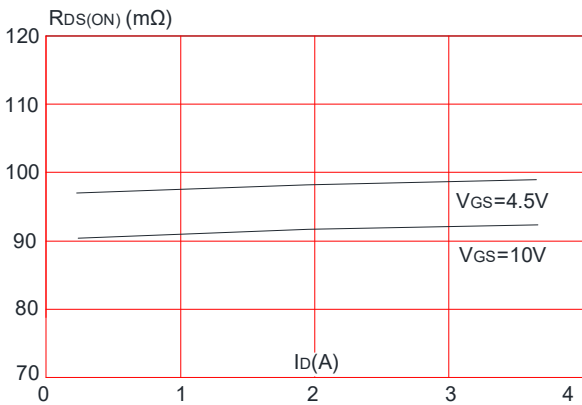


Figure 4: Body Diode Characteristics

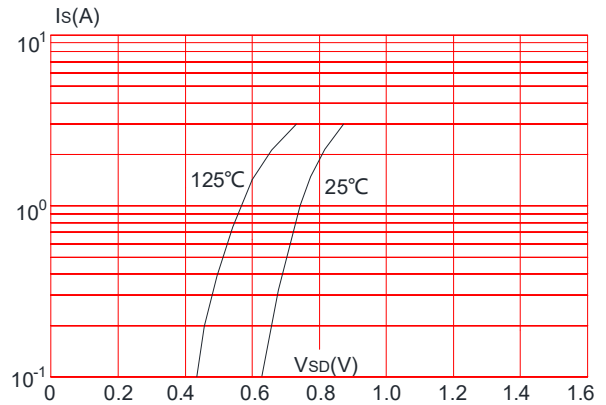


Figure 5: Gate Charge Characteristics

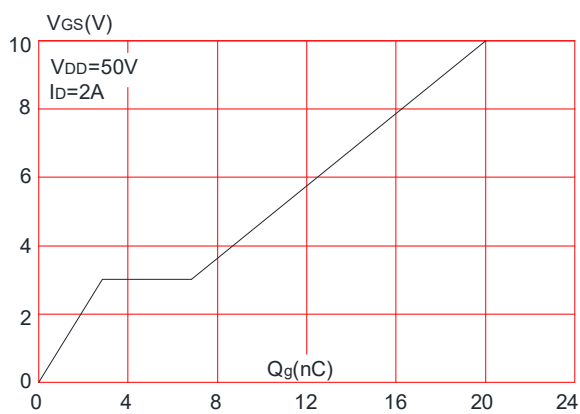
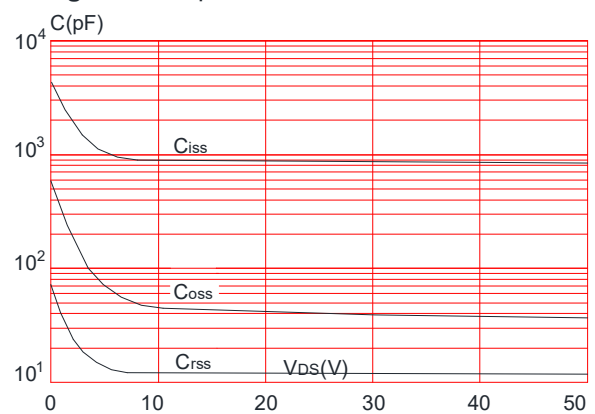


Figure 6: Capacitance Characteristics





JMTJ11DN10A

Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

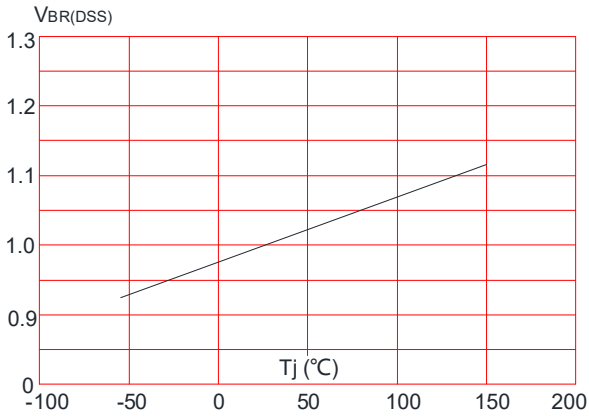


Figure 8: Normalized on Resistance vs. Junction Temperature

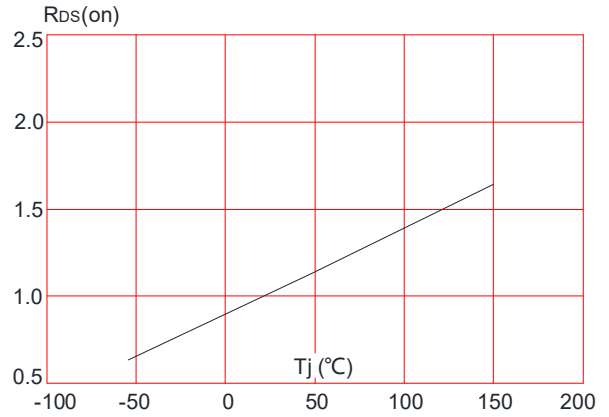


Figure 9: Maximum Safe Operating Area

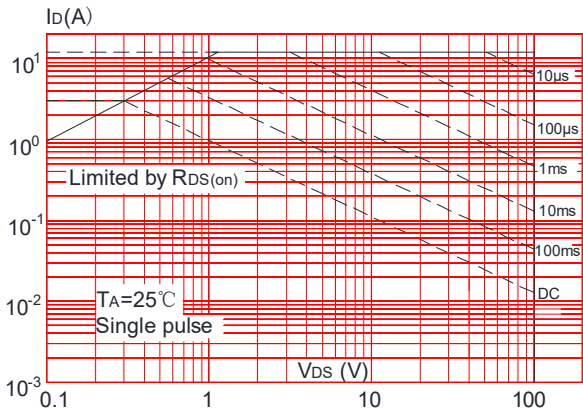


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

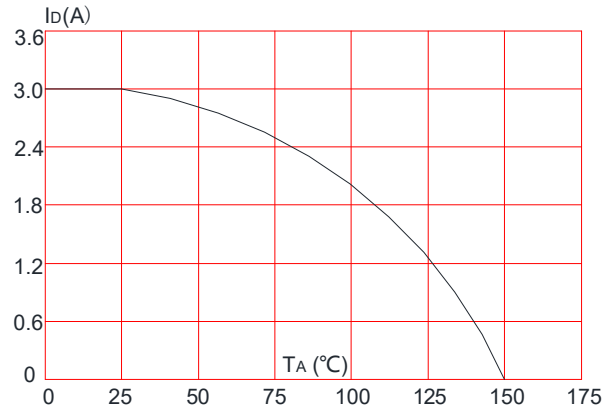
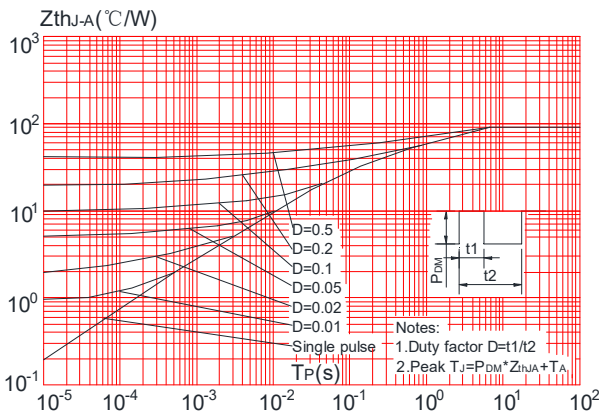


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

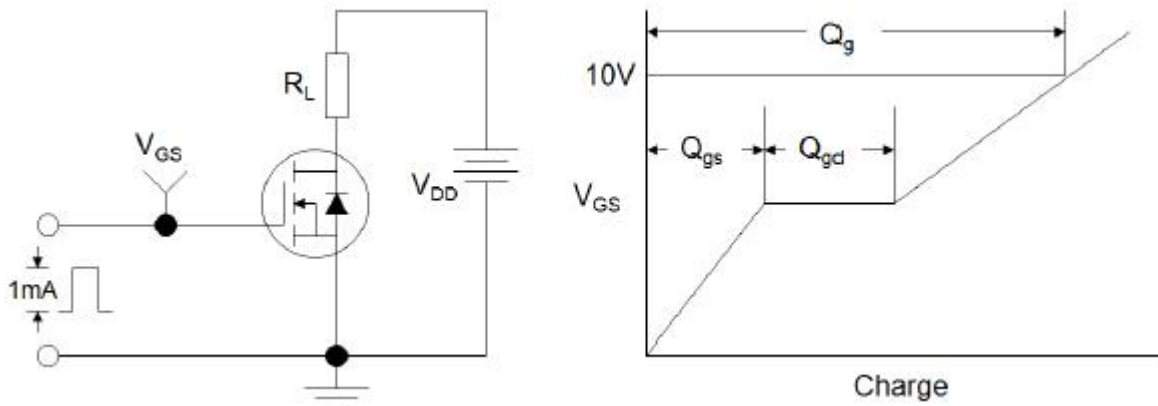


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

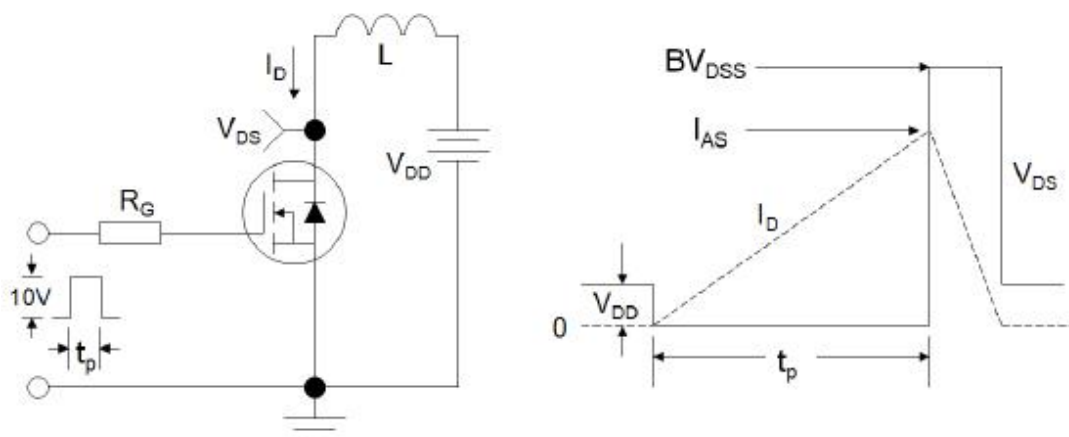
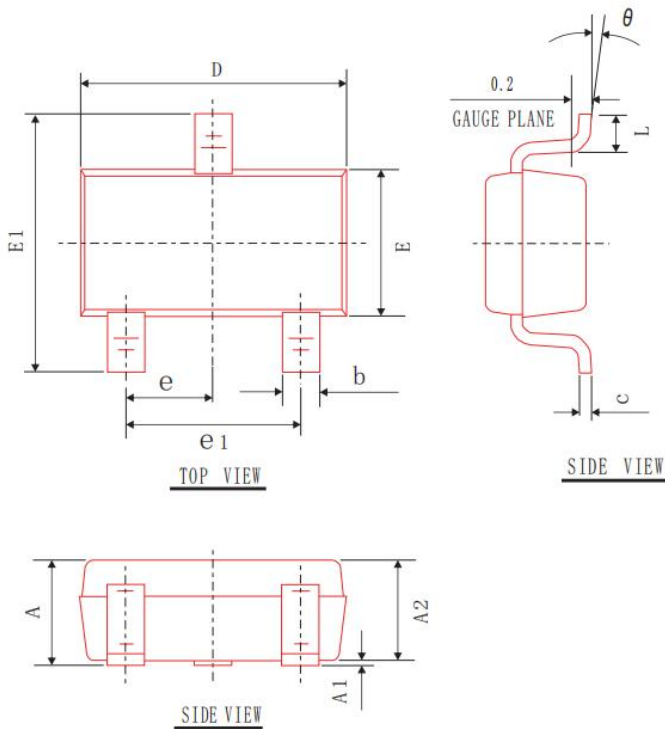


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOT-23-3L



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	---	---	1.30
A1	0.00	0.05	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.119	0.127	0.135
e1	1.80	1.90	2.00
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
L	0.30	0.45	0.60
θ	0°	4°	8°
e	0.95BSC		

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2022 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.