



Description

JMT P-channel Enhancement Mode Power MOSFET

Features

- $V_{DS} = -30V$, $I_D = -75A$
 $R_{DS(ON)} < 5.4m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 9.1m\Omega$ @ $V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

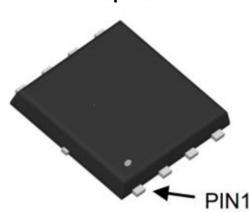
Application

- PWM Applications
- Load Switch
- Power Management

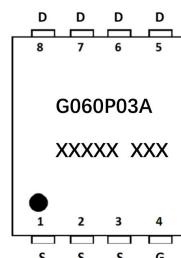
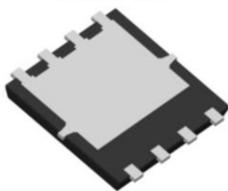


100% UIS TESTED!
100% ΔV_{ds} TESTED!

Top View

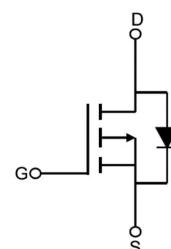


Bottom View



PDFN5x6-8L

Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
G060P03A	JMTG060P03A	TAPING	PDFN5x6-8L	13"	2500	25000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-75	A
		$T_C = 100^\circ C$	-49	A
I_{DM}	Pulsed Drain Current ^{note1}		-300	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		210	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	55	W
R_{eJC}	Thermal Resistance, Junction to Case		2.3	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D = -250\mu\text{A}$	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -30\text{V}$, $V_{GS}=0\text{V}$,	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$	-1.0	-1.6	-2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS} = -10\text{V}$, $I_D = -30\text{A}$	-	4.3	5.4	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$, $I_D = -20\text{A}$	-	7	9.1	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	6800	-	pF
C_{oss}	Output Capacitance		-	769	-	pF
C_{rss}	Reverse Transfer Capacitance		-	726	-	pF
Q_g	Total Gate Charge	$V_{DD} = -15\text{V}$, $I_D = -30\text{A}$, $V_{GS} = -10\text{V}$	-	30	-	nC
Q_{gs}	Gate-Source Charge		-	6	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	8	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -15\text{V}$, $I_D = -30\text{A}$, $V_{GS} = -10\text{V}$, $R_{\text{GEN}} = 2.5\Omega$	-	11	-	ns
t_r	Turn-on Rise Time		-	13	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	52	-	ns
t_f	Turn-off Fall Time		-	21	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	-75	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	300	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s = -30\text{A}$	-	-0.8	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD} = -15\text{V}$, $V_G = -10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$, $I_{AS} = -29\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

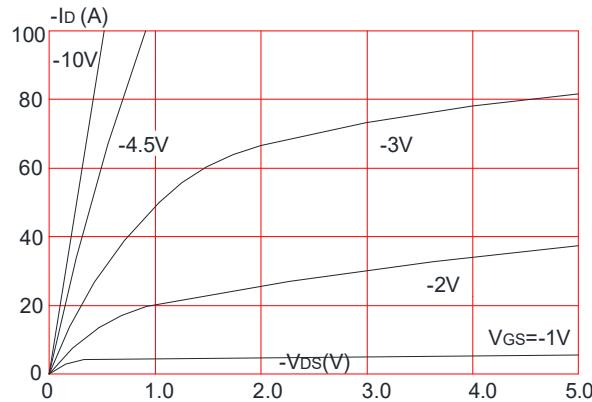


Figure 3: On-resistance vs. Drain Current

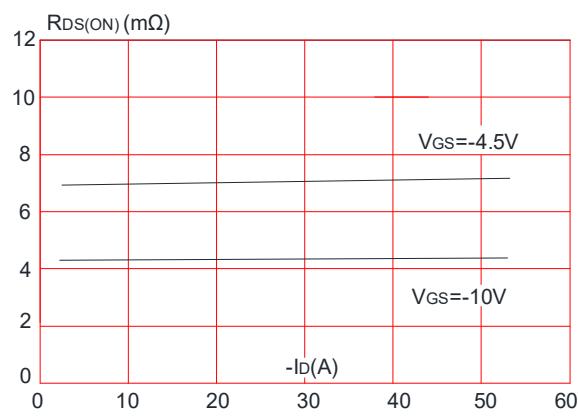


Figure 5: Gate Charge Characteristics

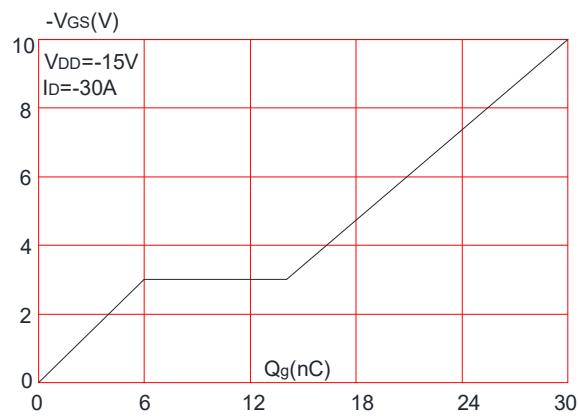


Figure 2: Typical Transfer Characteristics

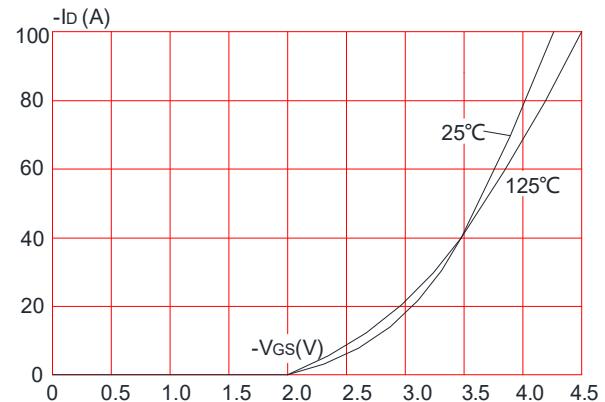


Figure 4: Body Diode Characteristics

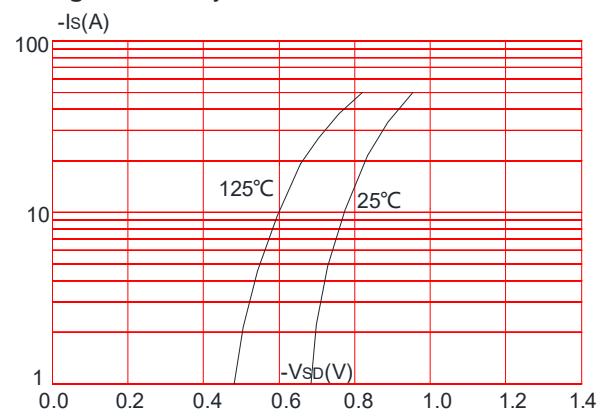


Figure 6: Capacitance Characteristics

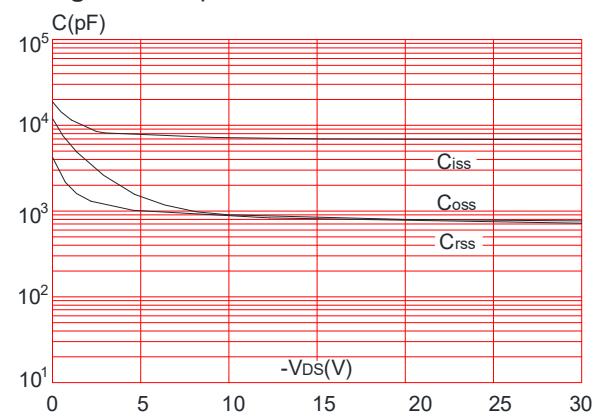


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

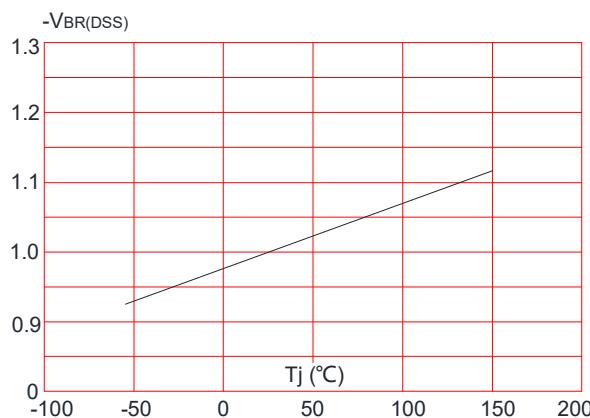


Figure 8: Normalized on Resistance vs. Junction Temperature

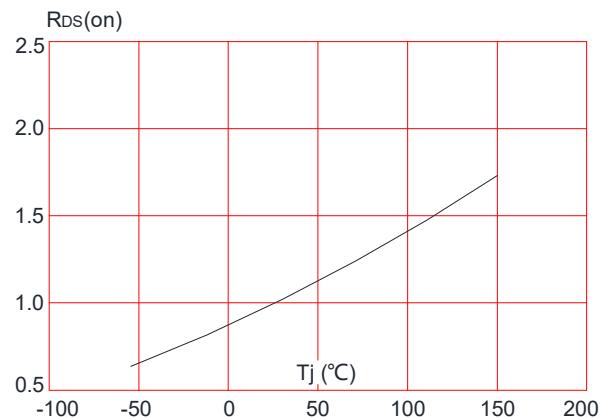


Figure 9: Maximum Safe Operating Area

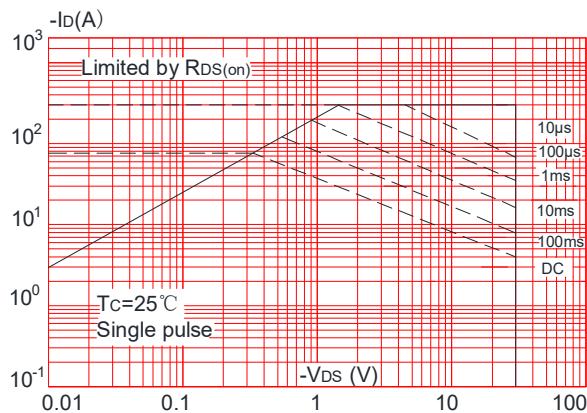


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

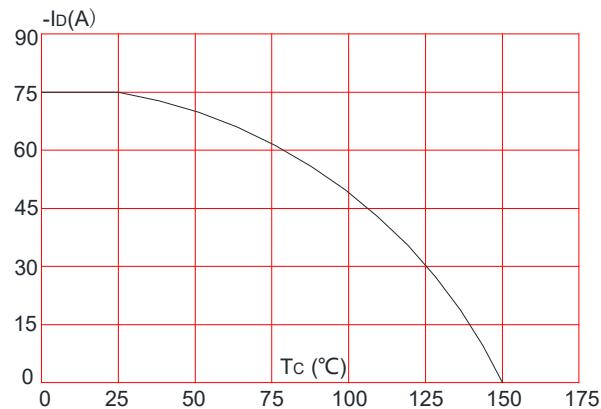
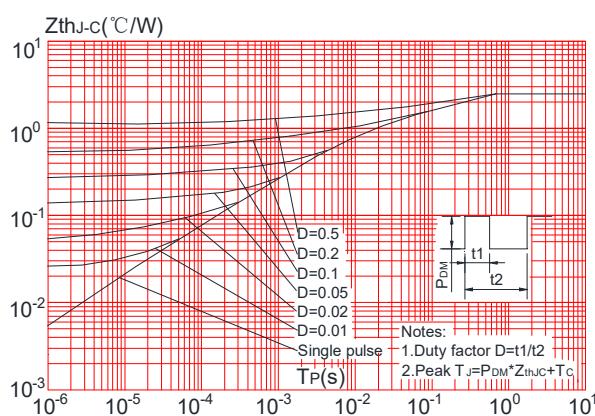
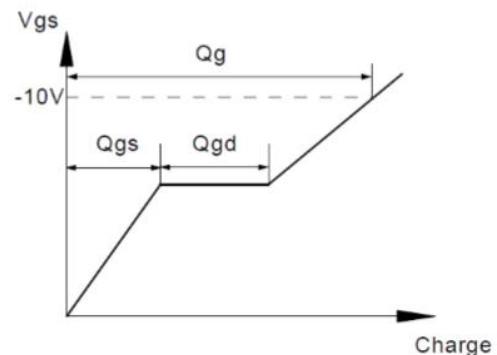
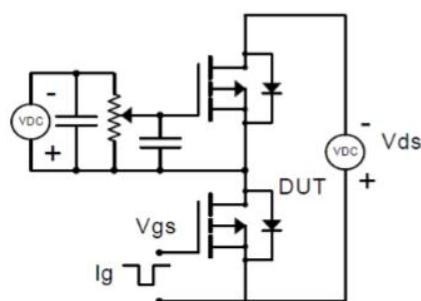


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

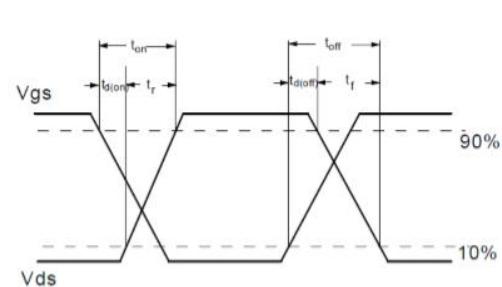
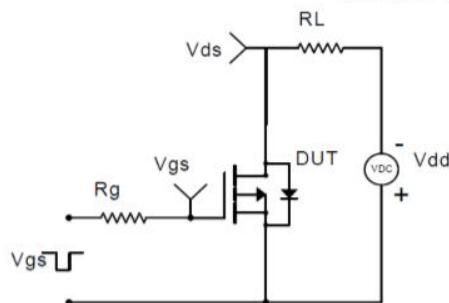


Test Circuit

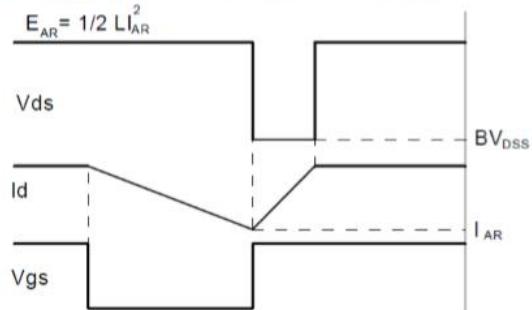
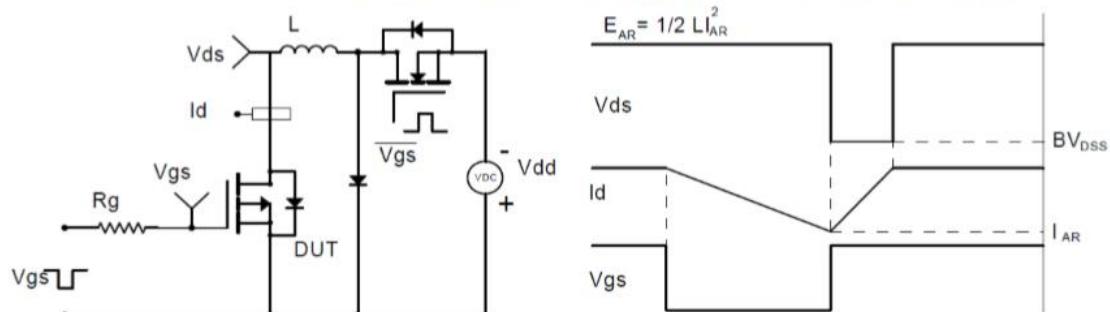
Gate Charge Test Circuit & Waveform



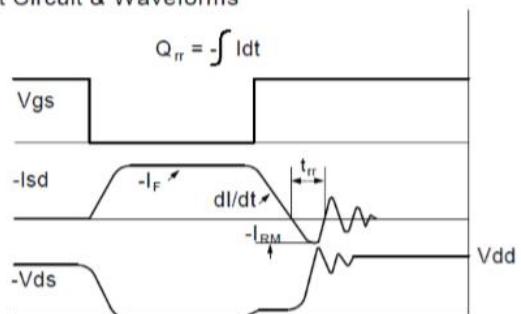
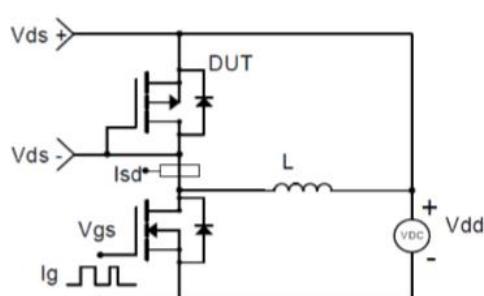
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

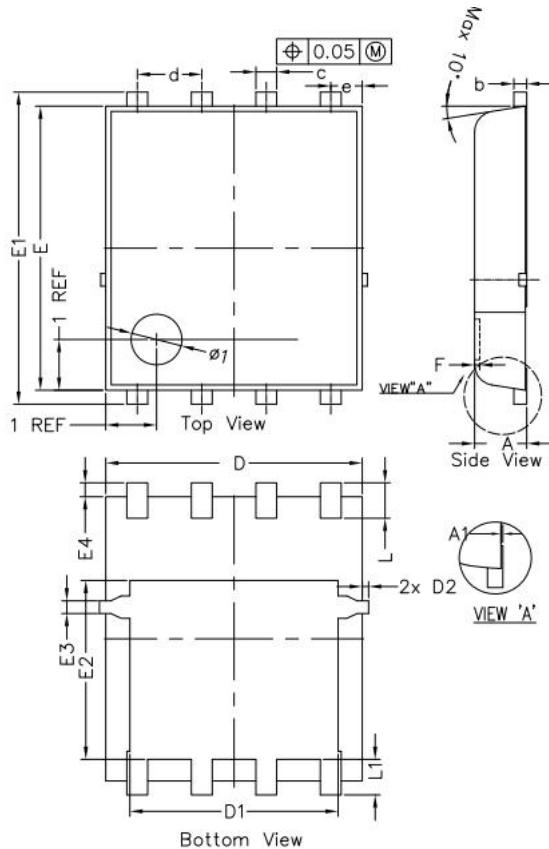


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data- PDFN5x6-8L



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	----	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d	1.27 BSC			0.050 BSC		
* D	4.950	5.050	5.150	0.195	0.199	0.203
D1	4.000	4.100	4.200	0.157	0.161	0.165
* D2	---	---	0.125	---	---	0.005
e	0.62 BSC			0.024 BSC		
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.425	3.525	3.625	0.135	0.139	0.143
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
* L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

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