PRODUCT CHANGE NOTICE
产品变更通知

PCN#编号:	PCN#20240918-001	**Date 日期:**	2024/09/18		
Subject 主题: 关于数字隔离器 CA-IS372XXS 产品系列封装焊线线材变更的 PCN PCN on the change of wire bonding material for Digital Isolator CA-IS372XXS series product					
Originator 发起人:	Taotao Gu	**Phone 电话:**	021-50838601	**Dept.部门:**	PE

Change Details 变更说明

Change Classification 变更等级: ☑ 一级变更 ☐ 二级变更 ☐ 三级变更 ☐ 四级变更

Change Type 变更类型:

☐ Wafer Fabrication 晶圆制造 ☑ Assembly 封装 ☐ Test 测试 ☐ Product Revision 产品改版

☐ Datasheet 产品规格书 ☐ End of Line 停产 ☐ Other其它

Description of Changes 变更描述:

数字隔离器 CA-IS372XXS 产品系列封装焊线线材变更

Digital Isolator CA-IS372XXS series product Wire bonding materials changes

变更前 before: 0.8mil 金线 0.8mil gold wire

变更后 after: 0.8mil 金钯铜线 0.8mil AuPdCu wire

Reason for Changes 变更原因:

1. 进一步优化成本结构，同时保持产品的高性能和可靠性。这一变更将有助于我们提供更具竞争力的价格，同时确保产品的质量和性能不受影响。
   To further optimize our cost structure while maintaining the high performance and reliability of our products. This change will help us to offer more competitive pricing while ensuring that the quality and performance of our products are not compromised.
2. 性能提升：金钯铜线在电学性能、热学性能等方面具有更出色的表现。例如，它可能具有更低的电阻，从而减少信号传输中的能量损耗，提高芯片的性能和稳定性。
   Performance enhancement: AuPdCu wire has better performance in terms of electrical and thermal properties. For example, it may have lower resistance, which reduces energy loss in signal transmission and improves chip performance and stability.

Impact of the change (positive or negative) on fit, form, function & reliability
变更（正面或负面）对外观、尺寸、功能和可靠性的影响:

1. 对产品外观，尺寸和可靠性方面均无影响。
   The change has no effect on the appearance, size and reliability of the product.
2. 对产品电性能均无影响。
   No effect on the electrical properties of the product

Products Involved 涉及产品型号:

- ✧ CA-IS3720HS；CA-IS3720LS；
- ✧ CA-IS3721HS；CA-IS3721LS；
- ✧ CA-IS3722HS；CA-IS3722LS；

Samples Status 样品状态:

客户有需求后 5 周提供样品。

Samples are available for delivery within 5 weeks after customer request received。

Implementation Date 实施日期:

2024/10/01

Appendix 附件:

1. 更新版可靠性报告 Updated Reliability Report

Chipanalog Approval/Comment: ☑ Approval ☐ Not approval ☐ Other	Date: 2024 年 9 月 18 日 Name/ title: Chen, Liang/Quality Director
Customer Approval/Comment: ☐ Approval ☐ Not approval ☐ Other	Date: Name/ title:

Remark: After Chipanalog notice of change is issued, for class 1 change, please review within 30 calendar days. For class 2 change, please review within 15 calendar days. If there is any problem, please feedback timely. If there is no feedback, you will agree to the change by default.
备注：川土变更通知发出后，一级变更请您在 30 天内进行评审，二级变更请您在 15 天内进行评审。若有问题，请您及时反馈。若未反馈，默认您同意变更。

For additional information regarding this change, contact your local sales representative or contact the PCN administrator at chenliang@chipanalog.com.
有关此更改的其他信息，请联系销售代表或 PCN 管理员：chenliang@chipanalog.com.

Reliability Test Report

Qualification Purpose： Device Change Qualification

Report Version: V1.0

Prepared by	Reviewed by	Approved by
胡静洁	唐坤	陈亮

Contents

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CA-IS372XXS series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family. This report is aimed to show the requalification data for CA-IS372XXS series chips, whose bonding wire is changed from Au to AuPdCu.

2. Part Number List

Package Type	**Part Number**
SOIC8-NB(S)	CA-IS3722HS/ CA-IS3722LS/ CA-IS3721HS/ CA-IS3721LS/ CA-IS3720HS/ CA-IS3720LS

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Package Information

Assembly site	SiMAT
FT site	SiMAT
Package	SOIC8-NB
Lead frame	Cu
Bond wire	20um AuPdCu
MSL level	MSL3

4. Reliability Requalification Plan

4.1. Qualification Vehicle

Qualification PN	CA-IS3722HS/3 lot

4.2. Qualification Test Plan

Stress	**Ref.**	**Abbv.**	**Conditions**	**Duration /Accept**
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)

High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to 150°C	1000 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C, 100% RH, 29.7 psia	96hrs/0 Fail
Biased Temperature/Humidity	JESD22-A110	HAST	130°C, 85% RH, 33.3 psia，$Vcc=Vcc_{max}$	96hrs/0 Fail
Bond Pull Strength	JESD22-B120	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	95% coverage

5. Reliability Test Results

5.1. Package Reliability Test Results

Package Type: SOIC8-NB				
Stress	**Condition**	**Duration**	**Sample size**	**Results**
PC	MSL 3	/	231*3 lot	Pass
HTSL	T_A = 150°C	1000 hrs	77*3 lot	Pass
TC	-65°C to 150°C	1000 cycles	77*3 lot	Pass
AC	121°C, 100% RH, 29.7psia	96 hrs	77*3 lot	Pass
HAST	130°C, 85% RH, 33.3 psia，Vcc_1=5.5V, Vcc_2=5.5V	96 hrs	77*3 lot	Pass
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass

6. Conclusion

CA-IS372XXS series chips with AuPdCu wire are requalified according to JEDEC standards.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	Change Log	Date
V1.0	Initial release	Sep, 2024